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B.E/B.Tech (Full Time) DEGREE END SEMESTER EXAMINATIONS, NOV/DEC 2011
ELECTRONICS AND COMMUNICATION ENGINEERING BRANCH
FOURTH SEMESTER (REGULATION 2008)
EC 9251–DIGITAL ELECTRONICS AND SYSTEM DESIGN

Time : 3 Hrs Max. Mark :100

Answer ALL Questions

PART-A (10 x 2 = 20 Marks)

1. Minimize the function using boolean algebra f = x(y+w'z) + wxz.
2. Determine the value of base x if $(211)_x = (152)_8$.
3. Write the characteristic equation for a JK flip flop and how could it be converted into a D flip flop?
4. Differentiate between Mealy and Moore models.
5. What is meant by "race" in sequential circuits?
6. Bring out the difference between synchronous and asynchronous sequential circuits.
7. Draw the basic logic diagram of a memory cell.
8. Bring out the difference between PAL and PLA.
9. Define noise margin in digital IC's.
10. Draw the logic diagram of a 3 input RTL NOR gate.

PART-B (5 x 16 = 80 Marks)

11. With neat sketches, briefly explain the working of a TTL gate with totem pole output and Tristate output configurations.

12.a)(i) With a neat logic diagram of a priority encoder, explain it's working. (8)
(ii) Design and draw the logic diagram of a full adder using only NAND gates. (8)

(OR)

12b)(i) Perform two level gate implementation of the function F = Σ(0,1,2,3,4,8,9,12) using NAND-AND gates. (8)
(ii) Implement the Boolean function F = Σm(0,3,5,6,8,9,14,15) with two 4 x 1 multiplexers. (8)

13.a)(i) Draw the logic diagram of D-type edge triggered flip flop and explain it's operation. (8)
(ii) With neat sketches, explain briefly the working of a 4-bit bidirectional shift register. (8)

(OR)

13.b) Design a synchronous counter which counts in the sequence 0,2,4,1,7,5,0.... using D flip flops. Draw the state diagram and logic diagram.

14.a) Design a negative edge triggered T flip flop which has two inputs, T(Toggle) and C(Clock) and one output, Q. The output state is complemented if T=1 and the clock C changes from 1 to 0. Otherwise, under any other input condition, Q remains unchanged. Draw the logic diagram of the designed circuit.

(OR)

14.b)(i) With appropriate examples, briefly explain the hazards in sequential circuits. (8)
(ii) An asynchronous sequential circuit has two internal states and one output. The excitation and output functions describing the circuit are as follows:

$$Y_1 = x_1 x_2 + x_1 y_2' + x_2' y_1$$
$$Y_2 = x_2 + x_1 y_1' y_2 + x_1' y_1$$
$$z = x_2 + y_1$$

Draw the logic diagram, transition table, output map and flow table of the circuit. (8)

(P.T.O)

15.a)(i) Implement the given functions using PAL

$F_1 = \Sigma m(0,1,3,5,7,9)$; $F_2 = \Sigma m(1,2,4,7,8,10,11)$ (10)

(ii) Write short notes on SRAM and DRAM. (6)

(OR)

15.b) With neat sketches, briefly explain the internal operation of the I/O block and configurable logic block of Xilinux 3000 series FPGA.