Register Number | | | | | | | | | | | |

B.E/B.Tech (Full Time) DEGREE END SEMESTER EXAMINATIONS, NOV/DEC 2011
ELECTRONICS AND COMMUNICATION ENGINEERING BRANCH
FOURTH SEMESTER (REGULATION 2004)
EC 281–DIGITAL ELECTRONICS AND SYSTEM DESIGN

Time : 3 Hrs Max. Mark :100

Answer ALL Questions

PART-A (10 x 2 = 20 Marks)

1. Convert the binary number 1011 to gray code.
2. Bring out the difference between minterms and maxterms.
3. What is meant by a tristate gate?
4. Define fan in and fan out.
5. Bring out the difference between Multiplexer and Encoder.
6. Draw the logic diagram of a half adder.
7. Write the characteristic equation for a JK flip flop and how could it be converted into a T flip flop?
8. What is meant by "ripple counters"?
9. What are the different modes of operation in asynchronous sequential circuits?
10. What is an essential hazard?

PART-B (5 x 16 = 80 Marks)

11. Explain all the methods used for race free assignment with an appropriate example for each.

12.a) Using tabulation method, simplify the function f= $\Sigma m(0,1,2,3,10,11,12,13,14,15)$.

(OR)

12.b)(i) Draw a logic diagram using NAND gates that implements the complement of the Boolean function $f = \Sigma m(0,1,2,3,4,8,9,12)$. (10)

(ii) Convert the hexadecimal number F3A7C2 to binary and octal. (6)

13.a) With neat sketches, briefly explain the working of TTL gate with totem pole output configuration and compare the same with open collector output configuration.

(OR)

13.b)(i) Draw the logic diagrams of 2 input CMOS NOR gate and 2 input CMOS NAND gate and explain their operation. (10)

(ii) List out the various characteristics of an IC. (6)

14.a)(i) Given a 32 x 8 ROM chip with an enable input, show the external connections necessary to construct a 128 x 8 ROM with four chips and a decoder. (8)

(ii) Implement the Boolean function $F = \Sigma m(0,3,5,6,8,9,14,15)$with a 8 x 1 multiplexer. (8)

(OR)

14.b)(i) Implement the given functions using PAL

$F_1 = \Sigma m(0,1,3,5,7,9)$; $F_2 = \Sigma m(1,2,4,7,8,10,11)$ (8)

(ii) Design and draw the logic circuit of a 2-bit magnitude comparator. (8)

15.a)(i) Draw the logic diagram of a master slave JK flip flop and explain it's working. (8)

(ii) With neat sketches, explain the operation of parallel in serial out shift register. (8)

(OR)

15.b) Design a synchronous counter which counts in the sequence 0,2,6,1,7,5,0.... using D flip flops. Draw the state diagram and logic diagram.