BE(Full Time) – III Semester- DEEE,COLLEGE OF ENGINEERING,

ANNA UNIVERSITY, CHENNAI-600 025

Time : 3 Hours | EE 9204- Digital System Design | Max Marks :100

Answer ALL Questions

1. Determine the base 'b' in each of the following cases : (i) $(361)_{10} = (551)_b$ (ii) $(859)_{10} = (5B7)_b$
2. Write the 8-bit signed magnitude, 2's compliment and 1's compliment form of the decimal number (-13)
3. Using the theorems of Boolean algebra simplify the following Boolean expression.f1(A,B,C,D) = B+BCD+B'CD+AB+A'B+B'C
4. Express the three-variable function f(A,B,C)=$\sum m(0,1)$ as a product of max terms
5. A combinational circuit is described by the equations
   $f_1(A,B,C)$ =ABC + A'B'C $f_2(A,BC)$ = A'B'C' + A'BC ; Design a circuit which will implement these two equations using a decoder with an AND gate external to the decoder.
6. Draw the circuit diagram of a S-R latch constructed using NAND gates and give the truth table.
7. Draw the logic diagram of an 3-bit asynchronous up counter.
8. Differentiate combinational logic and sequential logic circuits.
9. What are FPGAs? Mention few applications of FPGAs.
10. Mention any four MSI devices.

Part-B **5 x 16 =80**

11 (i)Design a three bit synchronous counter that goes through the following states 1,2,4,6,0... .
Use T FFs for realisation. (12)

(ii)Design a four bit binary down counter(ripple) (4)

12(a) (i) Consider the signed binary numbers : A = **0** 1000110 and B= **0** 1010011.
Perform the operations (A- B) and (-A + B) (3)

(ii) Prove the identity A'B + AB' = (A' + B')(A + B). (3)

(iii) Minimise the following function and implement the minimized function using only NAND gates: **f (A , B , C) = $\sum$m(0, 1,2, 3,4, 5, 6)** **(10)**

(OR)

12(b) (i) Using the Quine- Mccluskey method obtain all the prime implicants and the essential primeimplicants of the given Boolean function .Draw the logic diagram for the reduced xpression using NOR gates. $F(x1,x2,x3,x4)=\sum (0,1,2,3,4,8,10,13,14)$ (10)

(ii) Design a n- bit grey to n- bit binary code converter (6)

13(a) (i)Implement the following 4-variable functions using 3 x 8 decoders having active low outputs and NAND gates:

$f_1 = \sum m(0, 1, 3, 9, 12, 14)$

$f_2 = \sum m(5, 9, 10, 12, 13, 15)$

$f_3 = \pi M(0\ 3, 8, 11, 12, 15)$

$f_4 = \pi M(1, 2, 7, 8, 11, 12, 14)$ (8)

(ii) Construct a 5X32 decoder with four 3 x 8 decoders with enable inputs and one 2 x 4 decoder. (4)

(iii)Draw the internal circuit diagram of a 8 x 1 multiplexer and give the truth table. (4)

(OR)

13(b)(i) Implement the following 4-variable Boolean function using 4-input multiplexers and NAND gates: $f(A,B,C,D)=\sum m(0, 1, 3, 5, 6, 8, 9, 11, 12, 13)$ control variables A and B(6)

(ii) Give a brief description about PAL (4)

(iii) Implement the following 4-variable functions using a 16 x 4 ROM:

$f_1 = \sum m(0, 1, 3, 9, 12, 14)$

$f_2 = \sum m(5, 9, 10, 12, 13, 15)$

$f_3 = \sum m(0\ 3, 8, 11, 12, 15)$

$f_4 = \sum m(1, 2, 7, 8, 11, 12, 14)$ (6)

14(a) A sequential circuit has three D flip flops A,B,C and one input x . It is described by the following flip flop input functions $T_A = (B C' + B'C) x + (BC + B'C')X'$; $T_B = A + B$; $D_C = B$. The output $y = AB + X$. Derive the state table. Draw the state diagram for X= 0 and X=1 separately

(OR)

14(b) Design a 001 sequence detector . Use T flip flops for realization.

15(a) Design a synchronous modulo-12 counter using NAND gates and T flip-flops

(OR)

15(b) Analyse the circuit shown in Figure-1

(i) Determine the state table.

(ii) Determine the state diagram.

(iii) Use the state table to determine the output response to the input sequence X1X2 = 00, 01, 11, 10, 00, 01, 11, 01, 11, 10, 00.
Assume the initial conditionsare X1 = X2 = 0 and A = B =0.

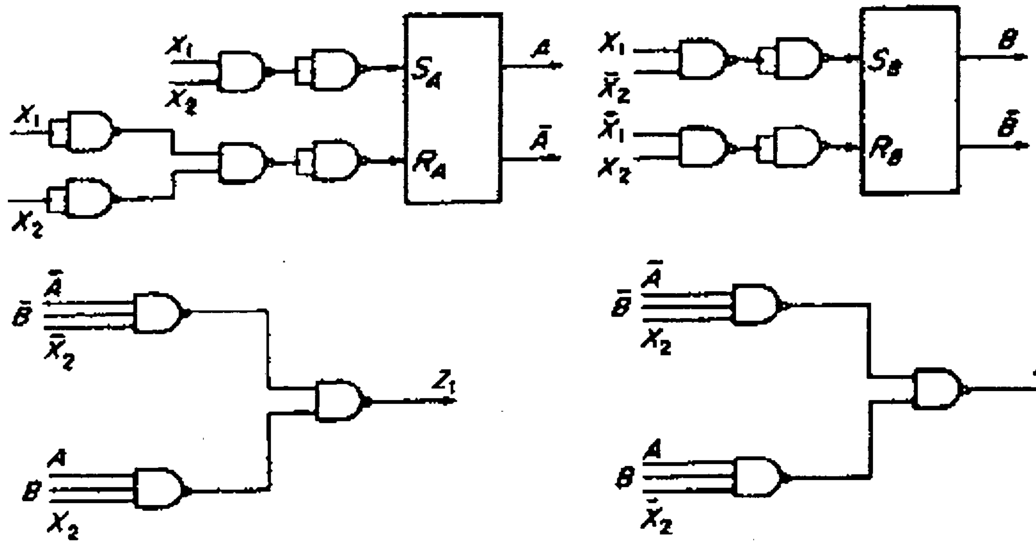

Figure -1