B.E./B.Tech. (FT) DEGREE END SEMESTER EXAMINATIONS, NOV/DEC 2011

Branch: Electronics and Communication Engineering

Fourth Semester

EC 9255 - Computer Architecture and Organization

Regulations 2008

Time: 3 Hours Max.Marks: 100

Answer ALL the Questions

PART – A (10 x 2 Marks = 20 Marks)

1. Describe the three methods of representing the negative numbers
2. What are the two task performed by an Instruction cycle
3. Draw the diagram to construct a Full adder using Half-adder
4. How do you compute the time taken by the CPU to execute a given program?
5. What is the speedup ratio of a pipeline over a nonpipelined machine?
6. Describe the following micro-operations

   PC <- MAR if Z = 1 else PC <- PC + 1
7. What are the characteristics of Memory devices?
8. Write the match logic to find a word "i" in an associative memory
9. What do you meant by Node Degree and Network Diameter?
10. What do you meant by super scalar processor?

PART – B (5X16 = 80 Marks)

11 (i) What are the factors to be considered when designing an instruction format? (4)

(ii) Explain any six addressing mode with examples in detail (12)

12 (a) Explain the n bit signed fixed-point division algorithm with a neat sketch by considering 10111 and 101 as example.

OR

12 (b) Draw the circuit diagram fir a 4-bit Ripple Carry Adder and explain how the delay time is reduced in the 4-bit Ripple Carry Look Ahead Adder.

13 (a) Explain the control points for a multiplier, and also design a microprogrammed control unit for it

OR

13 (b) Describe the addition of floating numbers and explain its pipelined implementation in IBM360

14 (a) Consider a cache consisting of 128 blocks of 16 words each, for a total of 2048 words and assume that the main memory is addressable by a 16 bit address and it consists of 4k blocks. How many bits are there in each of the TAG, BLOCK and word fields for different mapping techniques

OR

14 (b) (i) Explain the virtual memory address translation and TLB with necessary diagram. (8)

(ii) Draw the diagram to show the conversion of Virtual Address to Real address used in Intel Pentium Processor (8)

15 (a) With a neat diagram, explain any two techniques of Bus Arbitration in a multiprocessor environment

OR

15(b) Write Short notes on

(i) DMA

(ii) Interrupt

(iii) CISC Processor

(iv) Vector Processor

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