Reg. No. _____

B.E./B.TECH. (FULL TIME) DEGREE EXAMINATION APRIL/MAY 2011

Fifth Semester

Regulation 2004

Electronics and Communication Engineering

EC374 – Computer Architecture and Organization

Time: Three Hours Maximum: 100 Marks

Answer ALL questions

PART -A (10x2=20 Marks)

1) Mention the typical blocks in a computer organization.
2) Give the IEEE format of the floating point representation.
3) List any two advantages & disadvantages of a pipeline control.
4) Define a super scalar architecture. Give an example.
5) Draw the full adder circuit
6) Compare a combinational logic circuit and a sequential logic circuit.
7) Give the need of a cache memory.
8) What do you understand by interleaved memory?
9) What is the advantage of DMA transfer?
10) How do you generally classify interrupts?

PART – B (5 * 16 = 80 marks)

11.i) How do you classify the instruction type? Give example for each and explain. (8 Marks)

ii) Give the instruction formats of a typical processor with details of every byte in the instruction. (8 Marks)

12a) Explain the addressing modes with suitable examples for each. (16 Marks)

(Or)

b) i) Compare hardwired and microprogrammed control unit. (4 Marks)

ii) Draw the block diagram of a microprogrammed control unit and explain the operation. (12 Marks)

13a) What is the need for a carry look ahead adder draw the block diagram. Justify the need for such an adder with supporting proof. (16 Marks)

(Or)

b) Explain the various Hazards in a pipelined architecture suggest a remedy. (16 Marks)

14a) With a flow chart explain the floating point addition. Take into consideration a numerical example and explain the algorithm. (16 Marks)

(Or)

b) i) List the various cache memory organizations. (3 Marks)

ii) Explain any one of the above organization with necessary diagram compare it with other organizations. (13 Marks)

15a) i) Compare the different modes of DMA transfer. (4 Marks)

ii) Explain with a neat schematic how a CPU & a DMA work together in a design to perform a memory to hard disk transfer. (12 Marks)

(Or)

b) Write short notes on i) Superscalar Architecture

ii) RISC & CISC processor. (16 Marks)

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