End Semester Examinations - November 2011

BE(Full Time) – III Semester- DEEE,COLLEGE OF ENGINEERING,

ANNA UNIVERSITY,CHENNAI-600 025

Time : 3 Hours | EE 9204- Digital System Design | Max Marks :100

Answer ALL Questions

Part –A **10 X 2 = 20**

1. Realise a D FF using T flip flop and additional gates.
2. Construct a divide by 16 ripple down counter.
3. Design an even parity generator for three bit messages.
4. Implement the function F(x1,x2,x3,x4)= Σ(0,1,3,4,8,9,15) with an 8X1 multiplexer where the following variables are connected in the specified order to the selection lines s2,s1,s0 x1,x3,x4
5. Implement a half adder circuit with decoder and OR gates.
6. What are the modes of operation of asynchronous sequential circuits?
7. An 8 MHz square wave clocks a 5-bit ripple counter. What is the frequency of the last FF? What is the duty cycle of the output waveform.
8. Differentiate combinational circuits and sequential circuits
9. Reduce the Boolean function to one literal f(A,B,C) = A'B(D'+C'D) + B(A+A'CD)
10. What are FPGAs? Mention few applications of FPGAs.

Part-B **5 x 16 =80**

11. (i) Convert the number $[700]_8$ to base 4, base 12, base 16 and base 32 (4)

    (ii) Detect and correct the error in the following even parity Hamming coded message 1001001 (4)

    (iii) What are reflecting codes ? . Give examples. (4)

    (iv) Perform the subtraction using r's complement arithmetic $(0456)_{12}$-$(0234)_{12}$ and XS3 addition $(0902)_{10}+(0283)_{10}$ (4)

12. (a) (i) Consider the signed binary numbers : A = **0** 1000110 and B= **1** 1010011 where B is in 2's complement form. Perform the operations (A- B) and (-A - B) (3)

(ii) Prove that (x+y) + (x+z) = x'(y+z) (3)

(iii) Design a minimal two level gate combinational network that detects the presence of any of the six invalid code groups in XS3 code by providing a logic 1 output. Realize using NAND gates.(10)

(OR)

12(b) (i) Using the Quine- Mccluskey method obtain all the prime implicants and the essential prime implicants of the given Boolean function . Draw the logic diagram for the reduced expression using NOR gates. $F(x1,x2,x3,x4) = \Sigma(0,2,3,4,8,10,12,13,14)$ (10)

(ii) Design a n bit binary to n bit grey code converter (6)

13(a) (i)Given a 32x8 ROM chip with an enable input show the external connections necessary to construct a 128 x 8 ROM with four chips and a decoder (4)

(ii) Construct a 5X32 decoder with four 3 x 8 decoders with enable inputs and one 2 x 4 decoder (4)

(iii) List the PLA program table for the BCD –to-XS3 code converter circuit. (8)

(OR)

13(b)(i) Realize the functions given below using a PLA. Give the PLA table and internal connection diagram for the PLA:

$F1(a,b,c,d) = \sum (1,2,4,5,6,8,10,12,14)$

$F2(a,b,c,d) = \sum (2,4,6,8,10,11,12,14,15)$ (12)

(ii) Give a brief description about PAL (4)

14(a)A sequential circuit has three D flip flops A,B,C and one input x . It is described by the following flip flop input functions $D_A = (B C'+B'C) x + (BC+B'C')X'$; $D_B = A$; $D_C = B$. The output y =AB+X. Derive the state table. Draw the state diagram for X= 0 and X=1 separately

(OR)

14(b) Design a 1101 sequence detector . Use T flip flops for realization.

15(a) Design an asynchronous sequential circuit with two inputs x1 and x2 and one output z. Initially both inputs and output are equal to zero. When x1 or x2 becomes '1' z becomes 1. When the second input also becomes 1 the output changes to zero. The output stays at zero until the circuit goes back to initial state . Obtain the primitive flow table and design the circuit using SR latches.

(OR)

15(b) (i)An asynchronous sequential circuit has two internal states and one output. The excitation and output functions describing the circuit are as follows.

$Y_1 = x_1 x_2 + x_1 y_2' + x_2' y_1$

$Y_2 = x_2 + x_1 y_1' y_2 + x_1' y_1$; $z = x_2 + y_1$

Draw the logic diagram .Derive the transition table and anayse the circuit for critical and non critical race conditions. (12)

(ii) Investigate the transition table (given in Table 1)of an asynchronous circuit and determine all race conditions . Also determine whether there are any buzzer conditions. (4)

y_1y_2 \ x_1x_2	00	01	11	10
00	10	00	11	10
01	01	00	10	10
11	01	00	11	11
10	11	00	10	10

Table - 1