B.E. (FULL-TIME) DEGREE END SEM EXAMINATIONS
ELECTRICAL AND ELECTRONICS ENGINEERING
VIII SEMESTER
EE 518: VLSI DESIGN (R-2004)

Time: 3 Hours Max. Marks: 100

Answer ALL Questions

PART – A (10 x 2 = 20 Marks)

1 What are the advantages of SOI CMOS process?

2 What are the second order effects in a MOS Transistor?

3 State the significance of Lambda based rule.

4 What is Pass transistor?

5 Distinguish absolute clock skew and relative clock skew.

6 List the few applications of Tally circuits.

7 What factors determine the overall size of a PLA?

8 What is FPGA? Give the application of FPGA.

9 What is meant by continuous assignment statement in Verilog HDL?

10 Write the behavioral VHDL code for a full subtractor.

PART – B (5 x 16 = 80 Marks)

11 a (i) Describe n-well process in detail

(ii) Show the various components of nMOS transistor model.

12 a (i) Determine the pull-up to pull-down ration for an nMOS inverter driven by another nMOS inverter

OR

12 b (i) Draw and explain the lambda based rules for NMOS transistor region and contact cuts.

(ii) Draw the stick diagram and a mask layout for an 8:1 nMOS inverter circuit. Both the input and output points should be on the polysilicon layer.

13 a (i) What is Barrel shifter and discuss its SHIFT-1 &SHIEFT-2 operation

(ii) Construct a color-coded stick diagram to represent the design of the following integrated nMOS and CMOS structures and indicate pull-up/pull-down ratios in each case

- three-input NAND gate
- three-input NOR gate

OR

b (i) Draw and Explain CMOS 4:1 MUX with full pull-up and pull-down circuitry.

14 a (i) Write a brief note on PLA based finite state machine

(ii) Explain the NMOS NAND-NAND PLA realization with a neat stick diagram

OR

b (i) Draw and explain the clocked FPLA structure and compare it with PROM.

15 a (i) Explain : Bidirectional memory concept with VHDL code

(ii) Write the structural VHDL code for an 4bit Full adder.

OR

b (i) Write a VHDL function to convert an integer into a binary number
(ii) Explain a simple test bench for a bit comparator with necessary VHDL code