B.E. / B.Tech.(Full Time) END SEMESTER EXAMINATIONS, APR / MAY 2014
ELECTRONICS AND COMMUNICATION ENGINEERING
FOURTH SEMESTER – (REGULATIONS 2004)
EC 281 DIGITAL ELECTRONICS AND SYSTEM DESIGN

Time: 3 hr **Max. Marks: 100**

Answer ALL Questions

Part – A **(10 x 2 = 20 Marks)**

1. Convert 101100111_2 to gray code.
2. Obtain simplified POS using K-map for $f(A,B,C,D)=\sum(0,1,2,5,6,8)$.
3. Define fan out.
4. Draw the circuit diagram of a 3-input open collector TTL NAND gate.
5. Realize a full adder using 2-to-1 MUX.
6. What is an EAPROM?
7. Write the states in a 4-bit Johnson counter?
8. Distinguish between Moore and Mealy sequential networks.
9. Define dynamic hazard.
10. Define essential hazard.

Part – B **(5 x 16=80 Marks)**

11. Simplify using tabulation method $F(A,B,C,D) = \sum (0,1,2,7,8,9,10,11,14,15)$

12(a). Explain the working of a Totempole TTL NAND gate.

OR

12(b). Explain the working of CMOS inverter, NAND and NOR gates.

13(a). (i) Realize a 4-to-16 line decoder using 3-to-8 line decoders. (8)
(ii) Write the truth table and draw the logic circuit diagram of a 1 to 4 line deMUX. (8)

OR

13(b). Design BCD to Gray code converter. Use don't cares.

14(a). Design a counter with count sequence 0,1,2,5,4,3,7,6,0,1 and repeat using JK FFs.

OR

14(b). Draw the circuit of a Master-Slave JK FF using NAND gates only and explain its operation for J=K=1 by assuming an initial value Q=0.

15(a). Explain with the help of a suitable circuit that static-0 hazard occurs when there is a transition from 0 to 1 in one input variable.

OR

15(b). Obtain the primitive flow table for an asynchronous circuit that has two inputs D, P and one output Z where Z takes the value equal to the D input present at the moment when the input P is changing from 0 to 1. Two inputs D and P do not change simultaneously. Assume initial output as Z=0.

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