End Semester Examinations - April/May 2014 (R 2012)

BE(Full Time) – III Semester- Electrical and Electronics Engineering

College of Engineering, Anna University Chennai-600 025

Time : 3 Hours EE 8301 - Digital Systems Max Marks :100

Answer ALL Questions

Part –A 10 X 2 = 20

1. Realise an XOR gate using NAND gates.
2. Find the complement and dual of the Boolean function F(A,B,C) = AB + BC'
3. Draw the structure of an 8 X 4 ROM
4. What is a PLD ?
5. Find the difference using 15's and 16's complement arithmetic $(069)_{16}$-$(023)_{16}$
6. Implement the following function using only one 4:1 mux and minimum number of gates. $F(A,B,C,D) = \sum m(2, 3, 4, 5, 9, 11) + \sum d(0, 1)$
7. Explain the essential features of VHDL .
8. Draw the logic diagram of the T FF and write the Characteristic equation and Next state table.
9. Construct a decade asynchronous UP counter.
10. What is fundamental mode operation in Asynchronous circuits?

Part-B 5 x 16 =80

11. (i) Construct Hamming code for BCD 0110. Use even parity. (4)

    (ii) For the logic circuit shown in Fig-1, find out the logic function performed using Boolean theorems. (8)

(iii) Explain with example self-complementing codes. (4)

12 (a) (i) Given the Boolean function Y(A,B,C,D) =A + BC' +ABD' +ABCD

(*i*) Convert to standard SOP (4)

(*ii*) Reduce using K-map (4)

(*iii*) Construct circuit using NAND gates only. (2)

(ii) Find the reduced POS form using K-map

F(A,B,C,D) = πM(0,6,7,8,12,13,14,15). Implement using NOR gates . (6)

(OR)

12(b) (i) Convert to Canonical forms

(i) $F_1(X,Y,Z)= XY + Z$;

(ii) $F_2(X,Y Z) = (X + Y')(X'+Z)$; (4+4)

(ii) Using K map, simplify the following expressions and implement them using NAND gates

$F_1(A, B, C, D) = \sum m (1, 5, 6, 7,11,12,13) + \sum d (10,15)$

$F_2(A, B, C, D) = \sum m (0, 2, 5, 7, 8, 10, 13, 15)$ (4+4)

13(a) (i) Implement the function using only one 4 : 1 mux and gates.

$F(A, B, C, D) = \sum m (0, 2, 3, 6, 8, 9, 11. 13)$. (4).

(ii) Implement the following functions using active low decoder

$F_1(A, B) = \sum m (0, 1, 3)$,

$F_2(A, B) = \pi M (0, 2. 3)$ (Do not convert to SOP) (4)

(iii) Draw a ROM to implement the Boolean functions

F_1= ABCD+AB'CD'+ A'BC'D+ABC'D'

F_2= AB'+A'B (8)

(OR)

13(b) (i) Implement the following functions using PLA having 3 i/ps , 4 product terms and 2 outputs.

F1(A, B, C) = $\sum m (3, 5, 6, 7)$; F2(A, B, C) = $\sum m (0, 2, 4, 7)$. (8)

(ii) Implement the functions given in 13(b)(i) using ROM. (8)

14(a) A sequential circuit has three T flip flops A,B,C and one input x . It is described by the following flip flop input functions T_A= Ax' ;

$T_B = A\,x$; $T_C = B$. The output $y = A' + x$. Derive the state table. Draw the Mealy state diagram.

(OR)

14(b)(i) Design a synchronous counter that has the counting sequence 0,3,5,6,7,2,0 . Use D flip flops for realization. (8)

(ii) Derive the characteristic equation and excitation equation of J-K Flip flop. (8)

15(a) Design an asynchronous sequential circuit with two inputs x1 and x2 and one output z. Initially both inputs and output are equal to zero. When x1 or x2 becomes '1 ' z becomes 1. When the second input also becomes 1 the output changes to zero. The output stays at zero until the circuit goes back to initial state. Obtain the primitive flow table and design the circuit using gates. (16)

(OR)

15(b) (i) Explain the difference between asynchronous and synchronous sequential Circuits. (3)

(ii) What are the applications of Grey codes ? (3)

(iii) Explain the difference between stable and unstable states (3)

(iv) Convert the flow table shown in Figure-2 into a transition table by assigning the following binary values to the states : a = 00, b = 11 , c = 01. Assign outputs to the don't care states to avoid momentary false outputs. Derive the logic diagram of the circuit. (7)

	$x_1 x_2$			
	00	**01**	**11**	**10**
a	**a,0**	**b, -**	**c**	**a,1**
b	**a,-**	**b ,**	**b,**	**c,1**
c	**a,-**	**b, -**	**c ,1**	**c,1**

Figure-2