B.E. DEGREE END SEMESTER EXAMINATIONS, APRIL / MAY 2012
ELECTRONICS AND COMMUNICATION ENGINEERING
FOURTH SEMESTER – (REGULATIONS 2008)
EC 9251 DIGITAL ELECTRONICS AND SYSTEM DESIGN

Time: 3 hr Max. Marks: 100

Answer ALL Questions

Part – A (10 x 2 = 20 Marks)

1. Realize f(A,B,C,D) = Σ(1,3,5,7,9,11,13,15) using appropriate MUX without extra gates.

2. Implement a 2-level network for f(A,B,C,D)= Σ(9,12,13,14) using NOR only.

3. What is the application of ring counter?

4. Draw a 3-bit shift register configuration for parallel-in parallel-out data transfer.

5. Define critical and noncritical races.

6. List two situations in which asynchronous circuits are preferred.

7. What is the advantage of totempole TTL over open-collector TTL?

8. Compare Standard TTL and CMOS logic families in terms of fanout, propagation delay, power consumption and Noise margin.

9. What is the difference between PLA and PAL?

10. Compare static and dynamic RAMs.

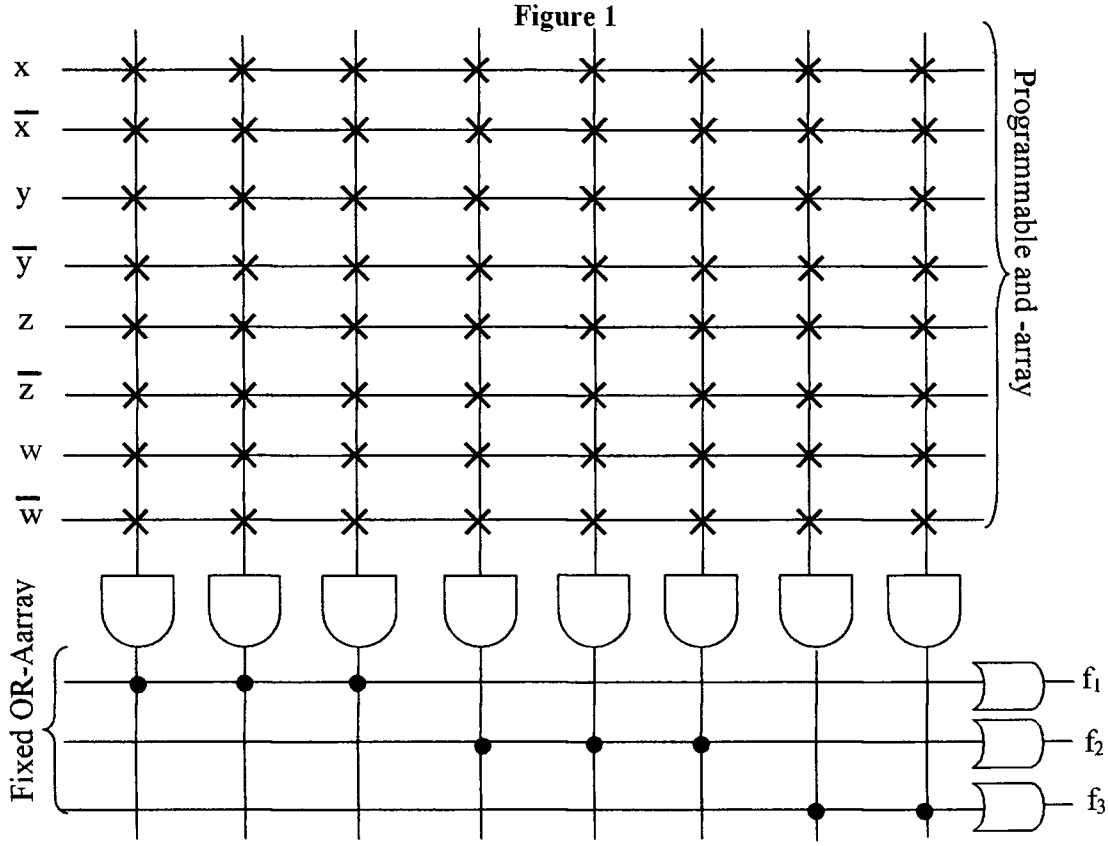
Part – B (5 x 16 = 80 Marks)

11.(i) Draw the logic diagram of a CLB and explain the architecture of a FPGA. (10)

(ii) Realize f1(x,y,z) = Σ(2,12,13), f2(x,y,z) = Σ(0,2,3,4,5,6,7,8,10,11,15), f3(x,y,z) = Σ(1,2,8,12,13) using the PAL in Figure 1. Crosses indicate fuses and dots indicate fixed connections. Removing a cross removes connection. (6)

(PTO)

Figure 1



12(a). Obtain simplified SOP using Quine-McClusky method for
F(A,B,C,D,E) = Σ(0,2,4,6,9,13,21,23,25,29,31)

OR

12(b). Explain the design of BCD adder.

13 (a). Explain the working of BCD ripple counter with timing diagrams.

OR

13(b). Design a single counter that counts up 0,1,2,3,0,1,2,3... if input X is 0 and counts down 3,2,1,0,3,2,1,0.... if input X is 1. Use T FFs.

14 (a). Explain static-0, static-1 and dynamic hazard with appropriate examples.

OR

14 (b). Obtain reduced pft for an asynchronous circuit that satisfies
(1) whenever inputs xy=00, outputs pq=00
(2) when x=1 and y changes from 0 to 1, outputs pq=01
(3) when y=1 and x changes from 0 to 1, outputs pq=10
(4) otherwise, the outputs do not change.

15 (a). Explain the working of tristate TTL gate.

OR

15 (b). Expalin the working of MOS and CMOS inverter, NAND and NOR gates.

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