Roll No. | | | | | | | | |

B.E / B.Tech (Full Time) DEGREE END SEMESTER EXAMINATIONS, NOV / DEC 2012
ELECTRONICS AND COMMUNICATION
Fourth Semester
EC 281 DIGITAL ELECTRONICS & SYSTEM DESIGN
(Regulation 2004)

Time : 3 Hours | Answer ALL Questions | Max. Marks 100

PART-A (10 x 2 = 20 Marks)

1. Convert 255_8 to decimal.
2. Express f(A,B,C)= **A+B'C** in terms of minterms.
3. Define fanout.
4. Draw the circuit diagram of an open collector TTL NAND gate.
5. Write the Boolean expressions for the 4-bit comparator signals (A>B) and (A<B) where A and B are the two 4-bit numbers.
6. How is the content in an EPROM erased?
7. What is the difference between a latch and Flipflop?
8. Draw the Moore state graph for recognizing odd parity in the sequence of input bits.
9. What is a stable total state?
10. Define Essential Hazard.

Part – B (5 x 16 = 80 marks)

11. (i) What are the assumptions in the preparation of a primitive flow table? (6)
    (ii)Explain cycle problem in asynchronous seq. circuits. (10)

12. a) Simplify using k-map f(A,B,C,D,E)=∑(2,6,8,9,12,13,18,22,24,25,28,29)

    OR

    b) Simplify using tabulation method f(A,B,C,D,E)=∑(2,6,8,9,12,13,18,22,24,25,28,29)

13. a) Explain the working of totempole TTL NAND gate.

    OR

    b) Explain the working of MOS inverter, NAND and NOR gates.

14. a) Explain the working of BCD adder that adds two decimal digits and a carry.

    OR

    b) (i)Implement f(A,B,C,D)=∑(0,1,2,4,5,6,8,9,12,13,14) using 8-to-1 MUX with B,C,D as selection lines. (8)
    (ii)Implement a full adder using 3-to-8 decoder. (8)

15. a) Design a synchronous counter to count 2,4,6,7,5,3,1,0,2,4,6,7,... repeat using JK FFs.

    OR

    b) Explain the data transfer techniques in a shift register.

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