Dept. of ECE, CEG Campus
End Semester Examination Nov 2012
B.E. (Full Time) (Arrears) VI Semester
EC 9075 CMOS Analog IC Design
Answer All Questions

Note: Assume all transistors are operated in saturation mode

Part A (10x2= 20 Marks)

Q1. For a resistance R, give the equivalent circuits and equivalent circuits and expressions for the thermal noise voltage and current.
Q2. For an NMOS transistor, state the conditions under which a transistor will operate in the saturation region.
Q3. Determine the small signal output impedance of the circuit in Fig.1.
Q4. Determine the small signal gain of the circuit in Fig.2
Q5. Determine the small signal gain for the circuit in Fig.3
Q6. Give the expression for the transonductance of a MOSFET and state the region of operation in this this expression is valid.
Q7. Explain why stability is not a problem in a single stage amplifier
Q8. Explain what is meant by CMRR.
Q9. Give the relationship between Id and gate to Vgs for the different regions of operation of a MOSFET.
Q10. Explain what is meant by body effect in a MOSFET device.

Part B (16x5=80Marks)

Q11. (i) Draw the small signal equivalent for the circuit and determine the voltage gain for the circuit in Fig.4

(ii) Give the expression for the output impedance of the circuit in Fig. 5 (derivation not required)

Q12. (a) Making use of symmetry considerations, determine the expressions for the differential gain and the common mode gain of the circuit in Fig.6.

OR

Q12 (b) Give the expressions for the output current, output impedance and the minimum output voltage for the circuit in Fig.Q7

Q13 (a) Give the expression for the differential gain for the circuit shown in Fig.8. Give also the expressions for the minimum and maximum ouptput voltages such that all transistors are in saturation.

OR

Q13 (b) Determine the expression for the equivalent output noise voltage for the circuit in Fig.9. Explain the main difference between white noise and 1/f noise.

Q14. (a) Define the terms gain margin and phase margins. Typically what values of phase margins are used and explain how reduction in phase margin affect the settling time.

OR

Q14 (b) Explain the need for Miller compensation. Explain two different schemes for Miller compensation.

Q15. (a) Explain, with the help of a circuit diagram, the operation of any one simple Bandgap Reference circuit.

OR

Q15 (b) Consider the block diagram in Fig.Q10. If H(s) is given by

$$H(s) = \frac{A_0}{\left(1 + \frac{s}{\omega_{p1}}\right)\left(1 + \frac{s}{\omega_{p2}}\right)}.$$

Determine the expression for the closed loop gain (Y(s)/X(s)) if $\beta = 1$.

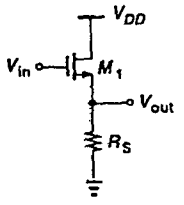

Fig.1

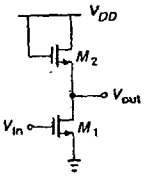

Fig.2

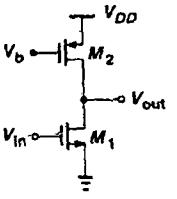

Fig.3

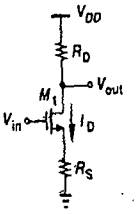

Fig.4

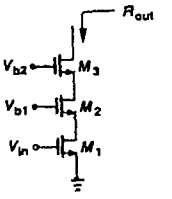

Fig.5

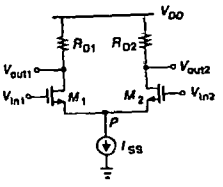

Fig.6

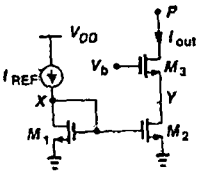

Fig. 7

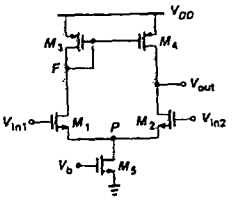

Fig.8

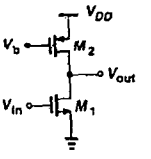

Fig.9

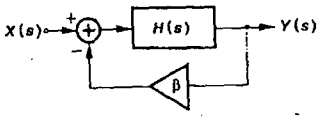

Fig.10