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B.E / B.Tech (Full Time) DEGREE END SEMESTER EXAMINATIONS, NOV / DEC 2012
ELECTRONICS AND COMMUNICATION ENGINEERING
Sixth Semester
EC9078 EMBEDDED AND REALTIME SYSTEMS
(Regulation 2008)

Time : **3 Hours** Answer **ALL** Questions Max. Marks: **100**

PART-A **(10 x 2 = 20 Marks)**

1. What are the functional requirements of embedded system?
2. Write ARM assembly code to implement the following C conditional:

```
if (x-y<3){
    a = b-c;
    x=0;
   }
else{
    y=0;
    d=e+f+g;
    }
```

3. Draw the state diagram for a bus read transaction.
4. Show the contents of the assembler's symbol table at the end of code generation for each line for the following program:

```
      ORG 200
p1    ADR r4,a
      LDR r0,[r4]
      ADR r4,e
      LDR r1,[r4]
      ADD r0,r0,r1
      CMP r0,r1
      BNE q1
p2    ADR r4,e
```

5. Bring out the difference between blocking communication and non-blocking communication.
6. What is meant by "re-entrant program"?
7. Draw the IP packet structure.
8. What is the necessity to have hardware accelerators in embedded system design?
9. What is meant by "feature creep"?
10. Give the necessity for memory management.

PART-B **(5 x 16 = 80 Marks)**

11. With neat sketches, explain the entire design of data compressor based on Huffman coding principle. Also illustrate the Huffman coding with an numerical example. (16)

12.a) With neat sketches, briefly explain about the address translation for a segment, address translation for a page and ARM two-stage address translation. (16)

(OR)

12.b)(i) Write an ARM assembly program for the following C code:

```
i=0; f=0;
while (i<N){
   f =f +c[i]*x[i];
   i++;
 }
```
(8)

(ii) Draw and explain the sequence diagram for transmitting a control input by a model train controller. (8)

13.a)(i) With a neat diagram, explain the principle of working of a DMA controller. (8)

(ii) Explain in detail about the domain testing for a pair of variables. (8)

(OR)

13.b)(i) With the help of a timing diagram, explain about the Extended data out (EDO) access in DRAM. (8)

(ii) Find the cyclomatic complexity of the CDFGs for the code fragment given below:

```
if (a<b) {
   if(c<d)
      x =1;
   else
      x =2;
} else {
   if (e<f)
      x =3;
   else
      x =4;
 }
```
(8)

14.a) With suitable examples, explain briefly about the co-operative multitasking and pre-emptive multitasking. (16)

(OR)

14.b) For the process shown below:

Process	Execution Time	Period
P1	1	4
P2	2	6
P3	3	12

Schedule using Rate Monotonic Scheduling (RMS) policy. Compute the schedule for an interval equal to the least-common multiple of the periods of the processes. Assume the time starts at t=0. (16)

15.a)(i) With a block diagram, briefly explain how the CPU cache can causes problems for accelerators and also suggest a technique by which the problem could be overcome. (8)

(ii) With a neat diagram of the CAN data frame format, briefly explain the working of the CAN bus. (8)

(OR)

15.b)(i) Explain in detail the working of Ethernet and also draw the flowchart for Ethernet CSMA/CD algorithm. (8)

(ii) Briefly explain about the message passing programming used in distributed embedded systems. (8)