Dept. of ECE, CEG Campus, Anna University
End Semester Examination Nov 2012 B.E(ECE) VII Semester (FT)
EC 9076 CMOS Analog IC Design II
Answer All Questions
Part A (10x2=20 Marks)

Q1. For Fig.1, give the expression for the voltage Vc across the capacitor C at the end of $\Phi 1$.

Q2. Explain briefly the tradeoffs involved in choosing between a binary weighted, thermometer coded and segmented DAC.

Q3. Explain the term 'idle tones' associated with sigma delta A/D converters.

Q4. Explain why it is preferable to use a preamplifier prior to a comparator.

Q5. If we control the S/H circuit using exact Dirac delta clock signals, there is no need to use anti-alias filter. Justify or refute this statement.

Q6. Which noise is removed by the decimation filter in a Sigma Delta converter.

Q7. What is the key factor that must decide the achievable SNR in a well designed pipeline ADC.

Q8. What is the main source of nonlinearity in a simple NMOS based Sample and Hold circuit.

Q9. Explain what factors can be used to reduce metastability in comparators.

Q10. In order to increase the maximum operating frequency of a Sample and Hold (S/H) circuit, one has to reduce the value of the hold capacitor C_H and reduce the ON resistance of the switch transistor. But this will then adversely affect some other characteristics of the S/H circuit. Explain.

Part B(16x5=80 Marks)

Q11. **(i)** Consider Fig.2 given below. Assume a unit amplitude sinusoidal signal (single tone) of frequency f_B is applied at input A. Sketch the Power Spectral Densities (PSD) at each of the points marked A,B,C,D,E,F and G. Assume a sampling frequency of $10f_B$. The sketch need only bring out the qualitative changes (if any) that take place in the PSD after each stage. You must show the quantization noise spectrum wherever applicable. You can make valid assumptions about the anti-alias filter.

(ii) Assume that the amplifier in the circuit shown in Fig.3 is ideal. Assuming two non overlapping clocks $\Phi 1$ and $\Phi 2$, express the voltage V_{out} measured at the end of $\Phi 2$ in terms of V_{in}

Q12.a. **(i)** Give the definitions for DNL and INL of a DAC. Express these quantities in terms of the standard deviation of the current element in a current steering thermometer coded DAC.

(ii) Fig.4 shows the circuit of a possible 'make before break' driver for a current steering DAC. Explain its principle of operation and state why this feature is desirable.

OR

Q12.b **(i)** For the basic comparator circuit shown in Fig.5, obtain the expressions for the output voltages $V_{out1}(t)$ and $V_{out2}(t)$ as a function of time. Assume that the initial voltages are denoted by $V_{out1}(0)$ and $V_{out2}(t)$.

(ii) Consider the comparator circuit shown in Fig.6. Assuming suitable values for Vin+ and Vin-, explain the operation of the comparator by sketching the following waveforms with respect to Clk and Clk. (1) gate voltages of M10 and M11 and (2) Out+ and Out -

Q13a. **(i)** Fig.7 shows the equivalent circuit of a track and hold circuit and can be used to highlight the effect of clock feed through. Due to clock feed through, the final output can be written in the form $V_{out} = (1+\varepsilon)V_{in} + V_{offset}$. Determine the expressions for ε and V_{offset} for the slow gating case and the fast gating case.

(ii) Explain the problem of charge injection. Explain how bottom gate sampling can help in reducing the problem of charge injection. Explain whether using the term 'bottom gate sampling' is appropriate.

OR

Q13.b Explain the operation of the circuit shown in Fig. 8. State your answer in the form of points, but you mast cover all the key steps in the operation.

Q14.a. Fig.9 shows the block diagram of a typical pipeline ADC.

(i).Derive the expressions relating the final Dout to the analog input voltage.

(ii).How many ADC and DAC are required in the block diagram shown.

(iii).In the above block diagram, should the resolutions (bits required) of all the ADCs and DACs be identical. If yes, justify. If not, which are the ones that can be different.

(iv) Indicate all those points in the block diagram where the signal is analog and where it is represented digitally. Hence indicate which operations in the block diagram are implemented in the digital domain and which ones in the analog domain.

OR

Q14.b Consider the circuit shown in Fig.10.

(i) For each of the clock phases Φ1 and Φ2, draw the equivalent circuit and indicate the voltages stored across the various capacitors.

(ii) Why are some switches shown as NMOS, while the others as transmission gates.

(iii) At what locations in the circuit are the final outputs obtained.

(iv) Assuming the opamp to be ideal, what is the expression for the differential gain of this circuit.

(v) For this circuit, comment on the impact of the opamp offset voltage on the output.

(vi) In order to reduce charge injection, indicate which clocks will have to be advanced.

Q15.a The circuit in Fig.11 can be used as single sigma delta quantizer. You have to sketch the equivalent circuit for each clock phase Φ1 and Φ2 separately. Explain very briefly how the functions of ADC, DAC and integrator are implemented during each phase and give appropriate expressions.

OR

Q15.b (i) The SQNR given by the formula 6n+1.2dB can be improved further by merely increasing the oversampling ratio OSR. Give the expression for the improvement obtained due OSR.

(ii) Derive the general expression for the Noise Transfer Function (NTF) and Signal Transfer Function (STF) for the Sigma Delta Converter shown in Fig.12.

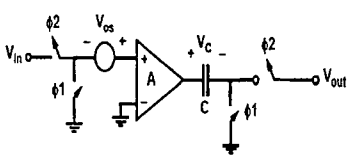


Fig.1

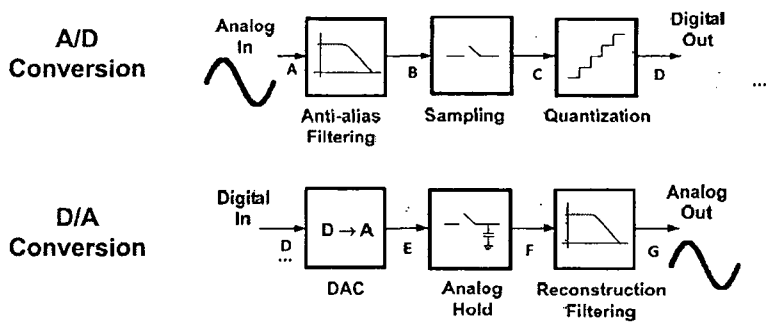


Fig.2

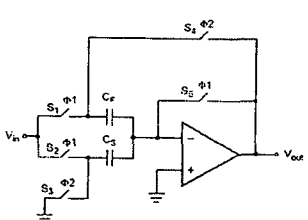


Fig.3

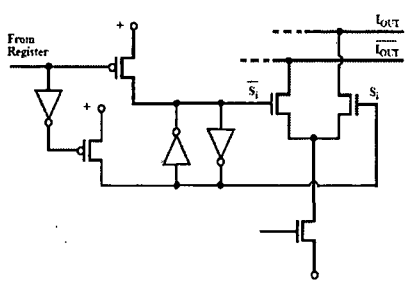


Fig.4

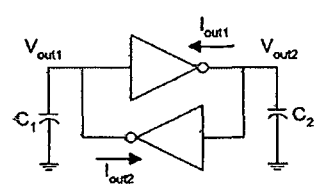
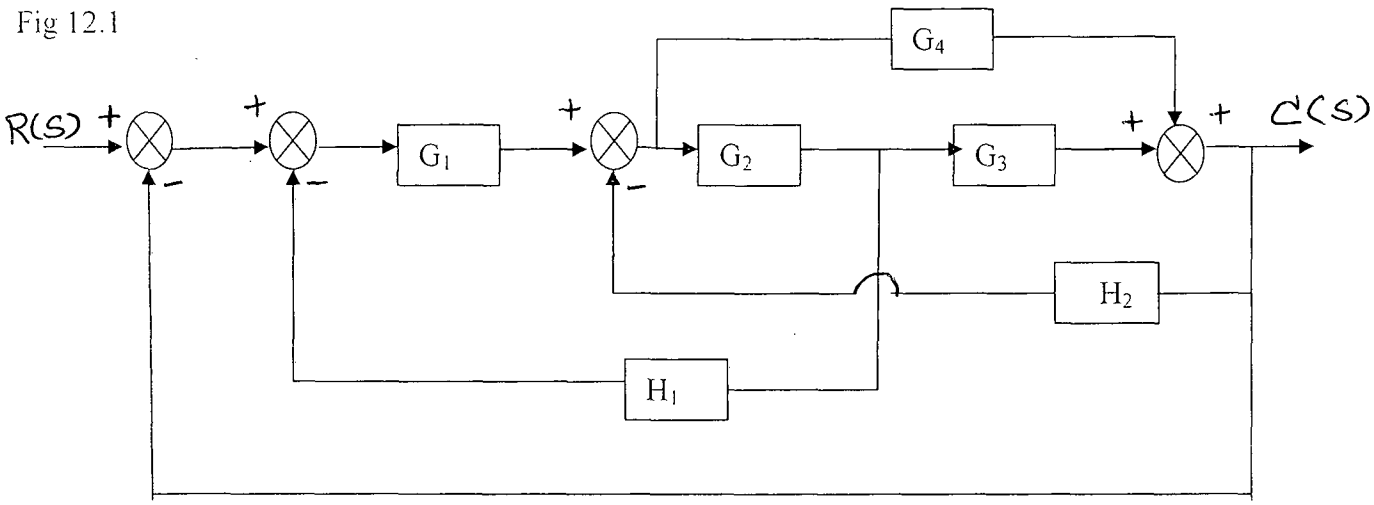


Fig.5

12. a). Find the transfer function for the given diagram by block diagram reduction method and verify the transfer function using Mason's Gain formula.

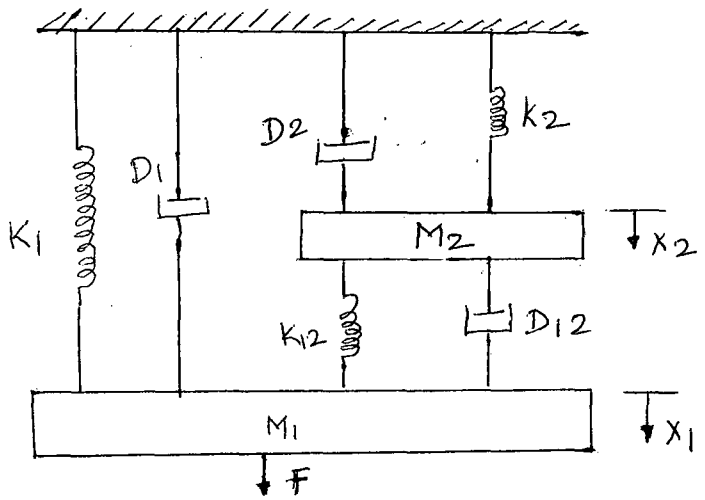
Fig 12.1



Or

b). Find the transfer function of the system shown in fig 12.2. Also determine the F-V and F-I analogies.

Fig12.2



13. a). i). A unity feedback control system is characterized by the following open loop transfer function $G(s) = \frac{0.4s+1}{s(s+0.6)}$. Determine its transient response for unit step input and sketch the response. Evaluate the maximum overshoot and the corresponding peak time. (10)

ii). Explain the response of undredamped second order system for unit step input with neccessary equation. (6)

Or

b).i) For a unity feedback control system the open loop transfer function, $G(s) = \frac{10(s+2)}{s^2(s+1)}$

Find (a) the position, velocity and acceleration error constants, (b) the steady state error when the input is R(s), where $R(s) = \frac{3}{s} - \frac{2}{s^2} + \frac{1}{3s^3}$. (10)

ii). Discuss the effect of PI controller of the system response. (6)

14. a). Given, $G(s) = \frac{Ke^{-0.2s}}{s(s+2)(S+8)}$. Find K so that the system is stable with, (a) gain margin equal to 2db, b) phase margin equal to 45^0.

Or

b). Consider a unity feedback control system having an open loop transfer function $G(s) = \frac{K}{s(1+0.2s)(1+0.05s)}$. Sketch the polar plot and determine the value of K so that (i) Gain margin is 18db (ii) Phase margin is 60^0.

15. a).i).The closed loop transfer function of control system is given by $T(s) = \frac{K}{s^4+6s^3+30s^2+60s+K}$. Determine the range in which K must lie for the system to be stable. (8)

ii).With the help of Routh-Hurwitz criterion comments upon the stability of the system having following characteristic equation $s^6 + 4s^5 + 11s^4 + 12s^3 + 26s^2 + 84s + 16 = 0$. (8)

Or

b). A unity feedback control system having an open loop transfer function $G(s) = \frac{K}{s(s^2+8s+32)}$. Sketch the root locus and determine the dominant closed loop poles with $\zeta = 0.5$. Determine the value of K at this point.