Roll No.									

B.E. / B.Tech (Full Time) DEGREE END SEMESTER EXAMINATIONS, NOV. / DEC. 2012

ELECTRONICS AND COMMUNICATION ENGINEERING BRANCH

EIGHT SEMESTER

EC 9045 – CAD for VLSI

(REGULATIONS 2008)

Time: 3 Hours Max. Marks:100

Answer All Questions

Part-A (10 x 2 = 20 Marks)

1) Define "data structure" and "algorithm".
2) What are the different complexity classes of algorithm? Arrange them in the increasing order of time complexities.
3) How is the placement algorithms grouped?
4) Write short notes on problem formulation.
5) Give the major objectives of floorplanning process.
6) Write a short on shape function in the floorplanning process.
7) List the Various Kinds of simulation process.
8) Prepare the comparison table between gate-level modeling and switch-level modeling.
9) What is meant by scheduling?
10) Why the high level synthesis model is necessary for hardware implementation process?

Part-B (5 x 16 = 80 Marks)

11)

(a) Describe in detail about the various VLSI design automation tools in the physical design cycle. (16)

12)

(a) Write and explain the pseudo code describe of Prim's minimum spanning tree algorithm. (16)

(or)

(b) Describe in detail about the Bellman-Ford algorithm. (16)

13)

(a) Describe in detail about the various channel routing models (16)

(or)

(b) Explain in detail about the Rectilinear Steiner-tree construction in global routing technique. (16)

14)

(a) Explain the basic version of Lee's algorithm for area routing. (16)

(or)

(b) Compute the positive co-factor of an ROBDD. List out the various factors. (16)

15.

(a) Mention the various hardware components that can be used by a system for the processing of high level synthesis. (16)

(or)

(b) Describe the Force directed scheduling algorithm. (16)