B.E./B.Tech.(Full Time) DEGREE END SEMESTER EXAMINATIONS, NOV / DEC 2012
ELECTRONICS AND COMMUNICATION ENGINEERING
VIII SEMESTER – (REGULATIONS 2008)

EC 9038 – VLSI SIGNAL PROCESSING

Time: Three hours | Max Marks: 100

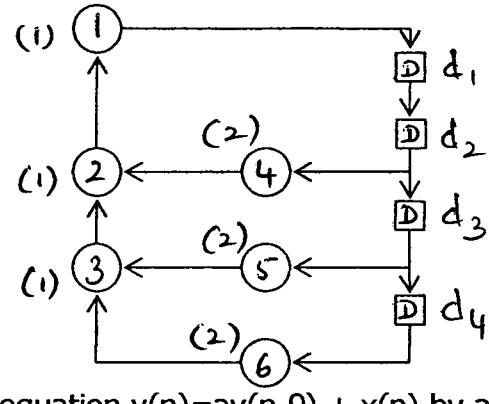
Answer ALL Questions

PART - A **(10 x 2 = 20 marks)**

1. Define iteration bound.
2. What are the disadvantages of pipelining?
3. What are the two steps in the unfolding algorithm?
4. Calculate the number of multipliers and adders in a 2-parallel fast FIR filter where the direct FIR has 100 taps.
5. Write the Lagrange interpolation formula.
6. Obtain the 4-level pipelined transfer function for $H(z)=\frac{1}{1-0.5z^{-1}}$ using power of 2 decomposition.
7. What are the characteristics of CSD numbers?
8. What is the decimal equivalent of the 2s complement number 1.1011?
9. What is numerical strength reduction?
10. What is a 2-phase clock?

PART - B **(5 x 16 = 80 marks)**

11. Calculate the iteration bound using LPM algorithm for



12 (a). Unfold the equation y(n)=ay(n-9) + x(n) by a factor J=2.

OR

12(b). Obtain a 2-parallel rank order filter with substructure sharing for a window size W=5.

13(a). Construct a 2 x 2 convolution algorithm using Cook-Toom algorithm with $\beta = 0, \pm 1$

OR

13(b). Design a 3-level pipelined architecture for the IIR filter y(n+1) = ay(n) + u(n).

14(a). Explain Lyon's precision multiplication.

OR

14(b). Obtain the CSD number for the 2's complement number 0.11011101

15(a). Explain the working of two-phase clock generator.

OR

15(b). What is wave pipelining and derive an expression for the clock period?

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