Registration Number :

END SEMESTER ARREAR EXAMINATION – NOVEMBER 2012

DEGREE	:	B.E.(Full Time) - Regulation 2008
BRANCH	:	Electronics and Communication Engineering
SEMESTER	:	Eight
CODE NO./ SUBJECT	:	EC 9031 – Satellite Communication

Duration : 3 Hours Max. Marks = 100

Answer ALL the questions.

PART A (10 x 2 = 20 marks)

1. List out the fundamental Newtonian equations that are used to derive the motion of a satellite in its orbit.
2. Given that the earth rotates once per sidereal day of 23 h 56 min 4.09 s, show that the radius of the GEO is 42,164.17 km.
3. What do you understand by Sun transit outage.
4. Draw the block diagram of a simplified double conversion transponder for operation at 14/11 GHz band.
5. Highlight the difference between QPSK and QAM modulation schemes.
6. What is the advantage of interleaving the data bits at the transmitter and de-interleaving them at the receiver end.
7. What is the necessity for unique word detection in TDMA based satellite systems.
8. Illustrate your understanding about spreading of a signal.
9. What do understand by Differential GPS.
10. Where does VSAT systems find their widest applications.

PART B (5 x 16 = 80 marks)

11. What is meant by DBS service and how does this differ from home reception of satellite TV signals in the C-band ? With the aid of a block schematic describe the functioning of the indoor receiving unit of a satellite TV / FM receiving system intended for home reception.

12a. What are Kepler's three laws of planetary motion. Give the mathematical formulation of Kepler's third law of planetary motion. What do the terms apogee and perigee mean when used to describe the satellite orbit. A satellite in an elliptical orbit around the earth has an apogee of 39,152 km and a perigee of 500 km. What is the orbital period of this

P.T.O

13 a) Draw with neat circuit diagram and timing diagram of BCD ripple counter and explain its operation

(or)

b) Reduce the number of states in the following state table and tabulate the reduced state table

Present state	Next state		Output Z	
	x=0	x=1	x =0	x=1
a	f	b	0	0
b	d	c	0	0
c	f	e	0	0
d	g	a	1	0
e	d	c	0	0
f	f	b	1	1
g	g	h	0	1
h	g	a	1	0

14 a) Implement the following functions using PLA

a) $f_1(A,B,C) = \sum(1,3,4,6,7)$

b) $f_2(A,B,C) = \sum(2,4,6,7)$

c) $f_3(A,B,C) = \sum(0,1,2,4,6,7)$

(or)

b) Explain with neat diagram the various modules present in FPGA XL4000 and its functions

15 a)i) Draw the circuit diagram and explain the operation of three input NAND gate using CMOS gate (10 marks)

ii) Draw the circuit diagram of CMOS inverter and explain its operation (6 marks)

(or)

b) i) Explain with neat diagram and working of two input NOR gate using RTL (6 marks)

ii) Explain with neat circuit diagram the operation of three state TTL gate (10 marks)