
B.E/B.TECH DEGREE END SEMESTER EXAMINATIONS, NOV/DEC 2011
INFORMATION TECHNOLOGY
THIRD SEMESTER – REGULATION 2008
IT 9401 COMPUTER ORGANIZATION

Time: 3 hr **Max.Marks:100**

Answer All Questions

Part – A (10X2 = 20 Marks)

1. Prove that x + xy = x in Boolean Algebra.
2. Whether 1's complement method of subtraction is convenient or 2's complement method of subtraction is convenient for a digital computer? Justify your answer.
3. Construct a 3 X 8 decoder using two 2 X 4 decoders.
4. Whether comparator is a sequential circuit or a combinational circuit? Justify your answer.
5. Draw the characteristics table of JK flip flop.
6. List the steps needed to execute the machine language instruction ADD LOCA, R0 in terms of registers PC, MAR, MDR, IR and ALU.
7. Characterize RISC machines in terms of the performance equation.
8. Write short notes on microprogrammed control unit.
9. Draw the hardware organization of a four stage pipeline.
10. Draw the typical memory hierarchy of a digital computer system.

Part – B (5X162 = 20 Marks)

11. i. Convert decimal +46 and +29 to binary using signed 2's complement representation and enough digits to accommodate the numbers. Then perform the binary equivalent of (+29)+(-49), (-29)+(+49) and (-29)+(-49). Convert the answers back to decimal and verify that they are correct. (8)

    ii. Simplify the Boolean function $F(A,B,C,D) = \sum (0,2,8,9,10,11,14,15)$ in sum of products form by means of a four variable Karnaugh map. Draw the logic diagram with (a) AND-OR gates (b) NAND gates. (8)

12 a. i. Design and implement a BCD adder. The detailed design procedure should include the table for the derivation of BCD adder and the block diagram of BCD adder. (8)

    ii. Design and implement a 4 bit comparator that is able to deal with three conditions namely less than, equal to and greater than. (8)

(OR)

12b. i. Explain the analysis of clocked sequential circuits in terms of state equation, state table and state diagram. (8)

    ii. Design and implement a universal shift register that possesses standard capabilities. (8)

13a. i. A two word instruction is stored in memory at an address designated by the symbol W. The address field of the first instruction (stored at W+1) is designated by the symbol Y. The operand used during the execution of the instruction is stored at an address symbolized by Z. An index register contains the value X. State how Z is calculated from the other address if the addressing mode of the instruction is direct, indirect, relative and indexed. (8)

ii. Draw the zoomed view of the processor and describe the function of various components. Also explain the bus structure. (8)

(OR)

13b. i. A relative mode branch type of instruction is stored in memory at an address equivalent to decimal 750. The branch is made to an address equivalent to decimal 500. Answer the following.

a. What should be the value of the relative address field of the instruction in decimal?
b. Determine the relative address value in binary using 12 bits.
c. Determine the binary value in PC after the fetch phase and calculate the binary value of 500. Then show that the binary value in PC plus the relative address in 12 bits is equal to the binary value of 500.

(8)

ii. Describe the straight line sequencing and branching of instruction execution with suitable examples. (8)

14a. i. Draw the basic organization of the hardwired control unit and explain its components. (4)

ii. Separate the decoding and encoding functions of the hardwired control unit and give some examples for the generation of control signals using logic gates. (6)

iii. Explain the register transfer of a general register Ri, scratch pad registers Y and Z in terms of input and output gating. Expand the arrangement for input and output gating for one register bit. (6)

(OR)

14b. i. Discuss the data hazard, instruction hazard and structural hazard of pipelining with suitable examples. (8)

ii. Modify the basic three bus organization of the data path of a processor so that it is able to deal with pipelining hazards. Explain the modified organization. (8)

15a. i. Discuss the usage of DMA controllers in a computer system with a neat block diagram. (8)

ii. Explain the centralized bus arbitration in DMA using a daisy chain arrangement of DMA controllers. (8)

(OR)

15b. i. Explain the direct mapping, associative mapping and set associative mapping functions of the cache memory. (8)

ii. Discuss the different replacement algorithms that are used in the maintenance of cache memory. (8)

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