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Roll Number: [ ]

UNIVERSITY DEPARTMENTS, ANNA UNIVERSITY, CHENNAI
B.E. DEGREE EXAMINATIONS, MAY 2013
R 2012, II SEMESTER

CS 8201 DIGITAL PRINCIPLES AND SYSTEM DESIGN

Time: Three Hours **Max. Marks: 100**

Answer All Questions

PART - A (10 X 2 = 20 Marks)

1. Perform the operation (22 – 32) using 2's complement arithmetic.
2. Show that a positive logic NOR gate is a negative logic NAND gate and vice versa.
3. State the distributive law of + over . and verify it using a truth table.
4. It is required to pass a resolution in a meeting that is attended by three people. The resolution is passed only when there is a 2/3 majority in favour of the resolution. Design a combinational circuit that will indicate whether the resolution is passed or not.
5. Show how a J-K flip flop can be constructed from a D flip flop.
6. Distinguish between the Mealy and Moore models of sequential circuits.
7. Mark the sable states and identify critical races, if any, in the following flow table.

	0	1
00	00	11
01	00	01
11	01	11
10	10	10

8. Provide the SR latch excitation table to be used for designing asynchronous sequential circuits.
9. Assuming Hamming code, generate the 3 parity bits for the data bits 1101. What does the received data 1110101 indicate?
10. Differentiate between a PLA and a PAL.

PART- B (5 x 16 = 80 Marks)

11. (i) Simplify $F(A,B,C,D) = \sum(0,6,8,13,14)$, $d(A,B,C,D) = \sum(2,4,10)$ using Karnaugh map. Draw the logic diagram using NAND gates only. (8)

    (ii) Reduce the following Boolean expression to minimum number of literals: A'B(D'+C'D) + B(A+A'CD). Indicate the theorems used. (4)

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(iii) Convert the Boolean expression (AB+C)(B+C'D) into SOP and POS forms. (4)

12. a) (i) Discuss the principle of operation of carry-look ahead adders. (10)
Derive the expressions and design a 4-bit carry-look ahead adder. Also calculate the delay for generating s_3 and c_4.

(ii) Design a combinational circuit that compares two 4-bit numbers to check if they are equal. The circuit output is 1 if the two numbers are equal and 0 otherwise. (6)

(OR)

b) (i) Design a single digit BCD adder circuit. Use 4-bit binary adder blocks. (6)

(ii) Write Verilog HDL code for a BCD adder. (6)

(iii) An 8X1 multiplexer has inputs A, B and C connected to the selection inputs S_2, S_1 and S_0, respectively. The data inputs I_0 through I_7 are as follows: $I_1 = I_2 = I_7 = 0$; $I_3 = I_5 = 1$; $I_0 = I_4 = D$ and $I_6 = D'$. Determine the Boolean function that the multiplexer implements. (4)

13. a) (i) Design a counter with the following repeated binary sequence: 0,2,4,6. Use J-K flip flops. (10)

(ii) Discuss the operation of a 4-bit ring counter. (6)

(OR)

b) (i) Discuss the design of a synchronous 4-bit up/down binary counter using T flip flops. (10)

(ii) A sequential circuit has two J-K flip flops A and B and one input x. The circuit is described by the following flip flop input equations:

$J_A = x$; $K_A = B'$; $J_B = x$; $K_B = A$.

Derive the state equations A(t+1) and B(t+1) by substituting the input equations for the J and K variables.

Draw the state table for the circuit. (6)

14. a) Merge the primitive flow table shown below. Proceed as follows:

- Find all compatible pairs using an implication table
- Find the maximal compatibles through a merger diagram
- Find the minimal set of compatibles that covers all the states and is closed

	00	01	11	10
a	a, 0	b, -	-, -	e, -
b	a, -	b, 0	c, -	-, -
c	-, -	d, -	c, 0	h, -
d	a, -	d, 1	-, -	-, -
E	a, -	-, -	f, -	e, 0
F	-, -	g, -	f, 0	h, -
G	a, -	g, 0	-, -	-, -
H	a, -	-, -	-, -	h, 0

(OR)

b) (i) An asynchronous sequential circuit has two internal states and one output. The excitation and output functions describing the circuit are (10)

$$Y_1 = x_1x_2 + x_1y_2' + x_2'y_1$$
$$Y_2 = x_2 + x_1y_1'y_2 + x_1'y_1$$
$$z = x_2 + y_1$$

Draw the logic diagram of the circuit. (3)
Derive the transition table and output map. (5)
Obtain a flow table for the circuit. (2)

(ii) What is a static hazard? Find a circuit that has no static hazards and implements the Boolean function

$F(A,B,C,D) = \sum(0,2,6,7,8,10,12)$ (6)

15. a) (i) Give the logic diagram of a basic RAM cell. Discuss how a 1K X 8 RAM can be constructed. Show all the connections and the decoding logic required. (10)

(ii) Discuss the characteristics of the different types of memories. (6)

(OR)

b) (i) Discuss the construction of a typical ROM. (10)
Show how a ROM can be used to implement a combinational circuit that has three inputs and produces an output that is twice that of the input.

(ii) Derive the PLA programming table for the combinational circuit that squares a 3-bit number. (6)

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