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B.E. DEGREE EXAMINATIONS, APRIL 2013
R 2008, III SEMESTER

CS 9204 COMPUTER ARCHITECTURE

Time: Three Hours **Max. Marks: 100**

Answer All Questions

PART - A (10 X 2 = 20 Marks)

1. State the CPU performance equation.
   Assume that a specific instruction takes 15 cycles and accounts for 20% of the instructions in a typical program, and the other 80% of the instructions require an average of 4 cycles for each instruction. What percentage of time does the CPU spend doing this instruction?
2. Discuss the concept behind the Booth's multiplication algorithm.
3. What are the issues to be considered when deciding on the types of addressing modes to be supported in the ISA of a processor?
4. Distinguish between vertical and horizontal microprogramming.
5. What is delayed branching? What are the different ways of filling instructions in the branch delay slots?
6. Give the state diagram of a 2-bit dynamic branch predictor and discuss.
7. Give the basic cell of an associative memory.
8. What is a TLB? How is it useful?
9. What are the functions to be performed by an I/O interface?
10. Distinguish between vectored and non vectored interrupts.

PART- B (5 x 16 = 80 Marks)

11. (i) Discuss the basic steps involved in the instruction cycle of a processor. For the single bus organization, write down the sequences of steps in order to do the following operation:
    ADD (R1)+, (R2) ,
    where the format is ADD src, dst and the instruction is one word only. (10)

    (ii) Discuss the concept of microprogramming. How does it compare with hardwired control? (6)

12. a) (i) Discuss the principle of operation of carry-look ahead adders. (10)
    Design a 64-bit adder that uses four 16-bit carry-look ahead adders along with additional logic to generate c_{16}, c_{32}, c_{48} and c_{64} from c_0 and the G_i^{II} and P_i^{II} variables. Also calculate the delay for generating s_{63} and c_{64}.
    (ii) Discuss the organization of a sequential binary multiplier. (6)

(OR)

b) (i) Discuss the operation of a floating point adder/subtractor unit. (10)
(ii) Discuss the IEEE representation used for floating point numbers. (6)

13. a) (i) Consider the following code that implements the operation Y = aX + Y for a vector length of 100. Assume that the multiply instruction has a latency of 6 and an add instruction has a latency of 2. Also assume that there are separate functional units for effective address calculations, for ALU operations, and for branch condition evaluation. For a **speculative** processor, create a table as indicated below showing the schedule for two iterations of the loop. Assume one CDB and that only one instruction can commit per clock cycle. (10)

Iter. No.	Instruction	Issue	Execute	Write	Commit	Comments
	loop:LD F0, 0(R1)					
	MULD F0, F0, F2					
	LD F4, 0(R2)					
	ADDD F0, F0, F4					
	SD 0(R2), F0					
	DSUBUI R1, R1, #8					
	DSUBUI R2, R2, #8					
	BNEZ R1, loop					

(ii) What is the need for dynamic scheduling?
Discuss the book keeping done by the Tomasulo's dynamic scheduler. (6)

(OR)

b) (i) What are the different types of hazards that might arise in a pipeline? (10)
Point out ways of handling them.
(ii) Discuss the concept of loop unrolling and how the compiler uses this technique to exploit ILP. (6)

14. a) (i) Compare and contrast the various mapping techniques used in cache memories. (10)
A computer system has a main memory consisting of 64M words.
It also has a 64K-word cache organized in the block-set-associative manner, with 4 blocks per set and 64 words per block. Calculate the number of bits in each of the TAG, SET and WORD fields of the main memory address format.

(ii) Discuss any four techniques used for improving the performance of cache memories. (6)

(OR)

b) (i) Discuss the concept of virtual memory and show how paging is implemented. (10)

(ii) List down the various types of memories used in computer systems and discuss their characteristics. (6)

15. a) (i) What are the different methods of transferring data between the processor and the peripheral devices? Discuss in detail. (10)

(ii) Distinguish between memory mapped I/O and I/O mapped I/O. (6)

(OR)

b) (i) What is the need for standard I/O interfaces? Discuss in detail the PCI or USB interface. (10)

(ii) Assuming that the processor has only one interrupt request line, discuss any two ways of handling multiple devices requesting interrupt service. (6)

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