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B.E. (Full Time) Degree End Semester Examinations, APR/MAY 2012

ELECTRICAL & ELECTRONICS ENGINEERING,

Fourth Semester – (Regulation 2008)

EE 9252 MICROPROCESSORS AND MICRO CONTROLLERS

Time : 3 hr Answer ALL questions Max. marks : 100.

PART – A (10 x 2 = 20)

1. If 'CALL, RET' instruction pair were not available in 8085, how would you manage writing subroutines? Remember that the execution control should return to the instruction next to the corresponding calling point in the main program.
2. List down the flags available in 8085? Which of them is/are not affected by the execution of the following instructions: INR B and CMA.
3. Show the decoding hardware necessary to interface a 2Kbyte sized EPROM to the 8085 with a required memory mapping of 5000 – $57FF_H$?
4. How would you store the contents of the (8085) stack pointer onto the top of the stack? Remember that the instruction PUSH SP is *invalid* in 8085.
5. What do you understand by the term 'baud rate'? What are the popular values of baud rates employed in the RS 232 based serial communication with a computer?
6. What is the role for ICW3 of the programmable interrupt controller 8259?
7. Distinguish between the operations of LXI H,2300_H and LHLD 2300_H? Also identify the addressing mode used in each of these instructions.
8. Discuss the operation performed by the 8051 instruction MUL AB. How does this instruction affect the overflow flag?
9. What is/are the instruction(s) available in µC 8051 to make reference to a look-up table included as a part of the program code?
10. Suggest an 8051 based scheme for measuring the speed of a motor shaft? Assume that an arrangement of teethed wheel along with electro-magnetic pick-up is available.

PART – B (5 x 16 = 80)

11. Explain how the 20 bit long 'physical address' is evaluated jointly by the BIU and EU of µP 8086, considering typical addressing modes and related base/ index registers? Also explain the other roles of these units BIU and EU, along with a neat sketch of the functional block diagram of intel 8086.

12. a) i) Draw the timing diagram showing fetching and complete execution of the µP 8085 instruction MVI M,65_H. Assume that this instruction is fetched from memory location 4321_H and that (HL) = 5678_H.

ii) Along with a neat sketch of the functional block diagram / architecture, describe the salient features available in the 8-bit µP 8085. (8 + 8)

OR

b) i) Correct the mistake in the following delay subroutine of µP 8085. Also evaluate the count required to obtain a time delay of about 13 msec. Assume a µP clock frequency of 2 MHz.

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Delay :    LXI  B, 16-bit count
Repeat :   DCX  B
           JNZ  Repeat
           RET.
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ii) Using μP 8085 assembly language, write a time delay subroutine, which generates a delay of 13 msec. Use counter-0 of 8253 timer in 'reading on fly / latch on count' mode. Assume its input clock frequency to be 100 kHz.

iii) Using μC 8051 assembly language, write a time delay subroutine, which generates a delay of 13 msec. Use one of its internal timers in any suitable mode. Assume the crystal frequency to be 12 MHz. (5+5+6)

13. a) Along with relevant external hardware, internal block diagram and relevant control word formats, explain how keypad and displays have been interfaced to μP 8085 using 8279 in the μP kits. Also write a program segment which would display the messages 'E.E.E.' and 'ISbESt' alternately (in the μP kit that you have used in the laboratory).

OR

b) i) Write an assembly language program which receives the 8-bit number made available serially at the SID pin? Store the received byte at the memory location 4500_H. Assume that there is only one delay subroutine available providing delay for half bit-time.

ii) Draw the external hardware necessary to insert RST 3 instruction in response to INTA signal from the μP. Also briefly explain the working, with the aid of relevant timing diagram. (8 + 8)

14. a) i) Discuss a scheme for measuring the room temperature with a resolution of $1^{O}C$? Use ADC 0801 and LM 135 as temperature sensor.

ii) It is required to achieve a two-way/ staircase switch: If both S1 and S2 are ON or, if both are OFF, the LED is OFF. If exactly one of the two switches is ON, the LED should glow. Show how employing 8255 simplifies this work of interfacing the two switches and LED to the μP 8085? You may employ Pin portC_0 for LED connection, so that BSR mode can be employed for controlling the LED. (8 + 8)

OR

b) i)A thumb wheel switch is connected as the input device, and two number of 7-segment LEDs connected through 7447 decoders form the output device. Both these are interfaced to μP 8085 through 8255 PPI. Assume suitable port connection. 8255 PPI itself is required to be connected following peipheral mapped I/O with address range of F0- $F3_H$. Draw the hardware connections. Also write a program which reads in the BCD input from thumb wheel switch and displays the value of its square at the 7-segment displays. Use a look-up table for getting the square value.

ii) Write a program in μC 8051 assembly language, to transmit a byte of data employing its UART facility (mode-1). Also explain the usage of its internal timer in mode-2, required for bit-time delay. (8 + 8)

15. a) Along with external hardware/ power circuit and machine cross-sectional diagram, explain how a stepper motor interface can be controlled from μP 8085 or μC 8051.

OR

b) Along with a neat sketch of the functional block diagram / architecture, describe the salient features available in the 8-bit micro-controller 8051.
