B.E. (FULL-TIME) DEGREE END SEM EXAMINATIONS April/May2012
ELECTRICAL AND ELECTRONICS ENGINEERING
III SEMESTER (REGULATION 2008)
EE 9204: DIGITAL SYSTEM DESIGN

Time: 3 Hours Max. Marks: 100

Answer ALL Questions

PART – A (10 x 2 = 20 Marks)

1 Express the Boolean function F=xy+x'z in a product of maxterm form.

2 Design a combinational circuit with three inputs and one output. The output should be 1,when the binary value of the inputs is less than three. And 0 otherwise.

3 Construct a J K flip-flop using a D flip-flop.

4 What type of Register is needed to convert serial data to parallel and parallel data to serial

5 Write the differences between Synchronous and Asynchronous sequential Circuits

6

7 Describe the differences between a PLA and a PAL by using logic diagrams.

8 What is the noise margin for TTL? Explain its purpose

9 Draw a circuit to implement the following VHDL statement

A <= B1 when C1 = '1' else B2 when C2 = '1' else
B3 when C3 = '1' else '0' Where all the signals are of type bit.

10 Estimate how many AND gates and adders will be required for a 16-bit *16-bit array multiplier.

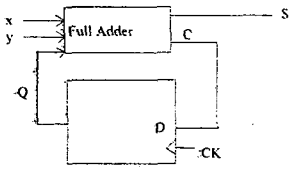
PART – B (5 x 16 = 80 Marks)

11 a (i) Given the Boolean function

F = xy'z+ x'y'z+ w'xy+wx'y+wxy

- Obtain the truth table of the function.
- Draw the logic diagram using the original Boolean expression.
- Simplify the function to a minimum number of literals using Boolean algebra.
- Obtain the truth table of the function from the simplified expression
- Draw the logic diagram from the simplified expression and compare the total number of gates.

12 a (i) A sequential circuit has one flip-flop Q, two inputs x and y, and one output S. It consists of a full adder circuit connected to a D flip-flop as shown in the figure below. Derive the state table and state diagram of the sequential circuit.



OR

b (i) A PN flip-flop has four operations: clear to 0, no change, complement, and set to 1, when inputs P and N are 00,01,10 and 11 respectively.

- Tabulate the characteristic table
- Derive the characteristic equation
- Tabulate the excitation table
- Show the PN flip-flop can be converted to a D flip-flop

13 a (i) Find the Critical race-free state assignment for the reduced flow table shown in the following figure

	00	01	11	10
a	(a)	d	(a)	c
b	a	(b)	(b)	d
c	d	(c)	b	(c)
d	(d)	(d)	e	(d)
e	f	c	(e)	c
f	(f)	b	a	(f)

OR

b (i) An Asynhronous sequential circuit has two internal states and one output. The excitation and output functions describing the circuit are

$$Y_1 = x_1\, x_2 + x_1\, y_2' + x_2'\, y_1$$
$$Y_2 = x_2 + x_1\, y_1'\, y_2 + x_1'\, y_1$$
$$z = x_2 + y_1$$

- Draw the logic diagram of the circuit
- Derive the transition table and output map
- Obtain a flow table for the circuit
- Describe the behaviour of the circuit

14 a (i) Design a Synchronous sequential machine that will detect the input sequence 000, 010,101,001. When the correct sequence has been detected it causes an output Z_2 to go high. Any incorrect input sequence of four three-bit code words causes output Z_1 to go high. After an input sequence of four three-bit code words, cause the state machine to initialize in preparation of a new input.

- Determine the minimum EPROM size.
- Identify inputs and outputs for the EPROM.
- Construct the EPROM data table and
- Draw the logic diagram including EPROM used and the state variable ICs used.

OR

b (i) Sketch the circuit diagram for a TTL two input tri-state NAND gate. Identify the logic input and the control input. Explain the condition of each transistor in the circuit when the tri-state enable is active.

(ii) Explain the purpose of Darlington pair found in the top transistor position of the TTL totem pole for the high speed and schotty subfamilies

15 a (i) Write a VHDL module that describes a 16-bit serial-in, serial-out shift register with inputs Serial input(SI), Enable(EN), and Clock shifts on rising edge(CK) and a Serial output(SO). [12marks]

(ii) Write a VHDL Description of an S-R Latch using a process [4marks]

OR

b (i) Implement a 3-to-8 decoder using a LUT whose output should be an 8-bit unsigned vector. Give the LUT truth table and write the VHDL Code.

(ii) Write VHDL code that finds the largest integer in the array of 20 integers.

- using a FOR loop
- using a while loop