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B.E / B.Tech DEGREE END SEMESTER EXAMINATIONS, NOV/DEC 2013

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Semester IV

EC374/EC 9255-COMPUTER ARCHITECTURE AND ORGANIZATION

(Regulation -2004/2008)

Time: 3 Hours

Answer ALL Questions

Max. Marks 100

PART-A (10 x 2 = 20 Marks)

1. Draw the architecture of difference engine.
2. Describe the different level of obstruction of a system.
3. State modified booth's algorithm.
4. Explain co-processor.
5. Draw the general structure of Micro programmed control unit.
6. Draw the speedup formula for a pipeline computer.
7. Draw the architecture of 1D RAM unit
8. Define the three locality properties of memory system.
9. What is the need for bus arbitration?
10. When will be DMA and Interrupt are processed by CPU.

Part – B (5 x 16 = 80 marks)

11. a) Discuss the floating point representation for a single and double precision(8)
b) Describe the IAS architecture in detail with its instructions. (8)
12. a) State the difference between restoring and non restoring algorithm and explain with example.

OR

b) Explain the concept of pipeline with the floating point operations by considering IBM systems.
13. a) Design the control unit of GCD processor using classical method and differentiate it with one hot method.

OR

b) Write short note on i) Superscalar Processing ii) Nano Programming.
14. a) Explain memory address translation architecture used in Intel Pentium processor.

OR

b) What are the advantages of Mapping? Explain any two methods of Cache mapping.

15. a) Explain about bus arbitration and its types.

OR

b) Explain the types of interrupts.