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ANNA UNIVERSITY :: CHENNAI

B.E. / B.Tech. (Full Time) DEGREE END SEMESTER EXAMINATIONS, APRIL / MAY 2011

COMPUTER SCIENCE & ENGINEERING BRANCH

SECOND SEMESTER – (REGULATIONS 2008)

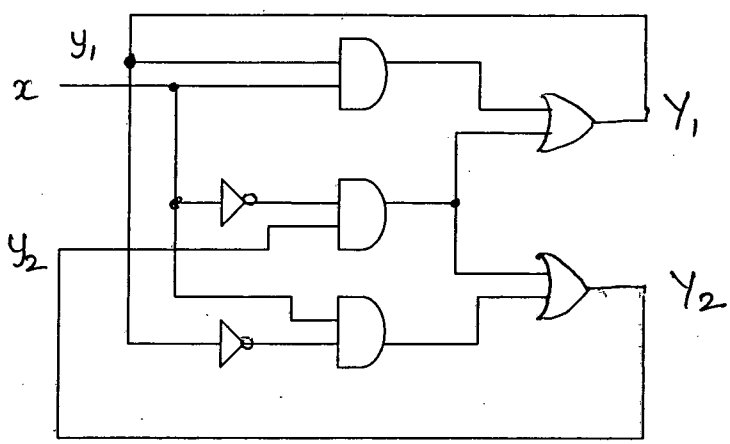
CS 9152 - Digital Principles and System Design

Time : 3 Hrs. **Max. Marks : 100**

Answer ALL Questions

PART – A (10 X 2 = 20 Marks)

1. Subtract using 2's Complement: 10101 from 110100.
2. Reduce the Boolean expression A'B (D' + C' D) + B (A + A' CD) to one literal.
3. Convert the following Boolean function to a form such that it can be implemented using only the NAND gates : F = ((AB) ' (CD) ')'.
4. Design a combinational circuit with three inputs and one output. The output is 1 when the input is a prime number. The output is otherwise 0.
5. Give the truth table and logic diagram for a 2-to-4 line decoder with active high enable input.
6. Draw the three major types of Combinational PLDs.
7. What is the indeterminate state of SR latch? How this could be eliminated by a D latch?
8. Give the excitation table of JK Flip Flop.
9. Give the transition table for the following circuit.



10. Brief on the types of hazards with respect to sequential circuits.

PART-B (5 x 16 = 80 Marks)

11. (i) Discuss the basic steps involved in the instruction cycle of a processor. Show the sequence of operations that take place in a single bus organization for the instruction

ADD ADDR, R2, # DATA

where the format is ADD dst, src1, src2. (10)

(ii) Discuss the concept of microprogramming. How does it compare with hardwired control? (6)

12. a. (i) Discuss the construction of a 4x4 array multiplier. (10)

(ii) What is a carry save adder? What are its advantages? (6)

OR

b. (i) Discuss the restoring division algorithm.
Simulate the same for the numbers 15 / 9. (10)

(ii) Discuss the operation of a floating point adder/subtractor unit. (6)

13. a. (i) Discuss the book keeping done by the Tomasulo's dynamic scheduling algorithm.

Schedule the following code assuming that the hardware has one integer unit (handles also all memory references and branches) with a 1-cycle execution latency, one Floating-Point Add/Sub unit with 2-cycles execution latency, two FP Mult units with an execution latency of 10 cycles, and one FP Div unit with a 40-cycle latency. (10)

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LD      F6  34(R2)
LD      F2  45(R3)
MULD    F0, F2, F4
SUBD    F8, F0, F2
DIVD    F10, F0, F6
ADDD    F6, F10, F2
MULD    F2, F0, F6
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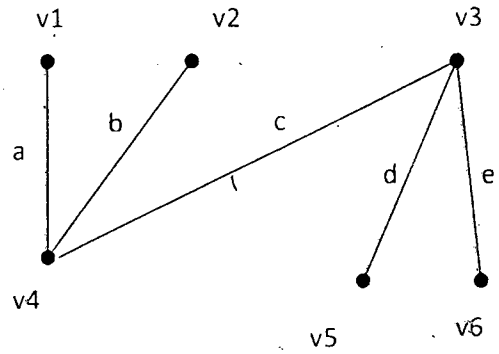
(ii) What is meant by delayed branching? Discuss the different ways by which the compiler fills the branch delay slots. (6)

13. a) (i) Check whether the following statement is true or false. Justify your answer by giving a short proof or counter example. "Every bipartite graph need not be a tree." (8)

(ii) In the graph given below give the following with justification: (8)

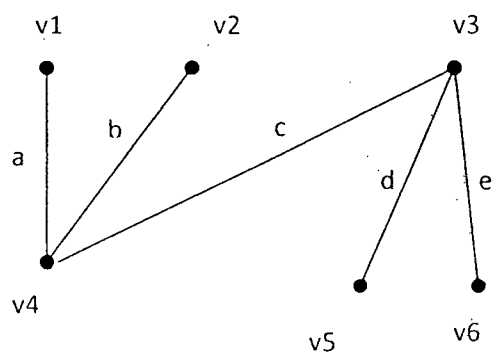
I) A matching of maximum size
II) A minimal dominating set
III) An independent set of vertices of maximum size
IV) A minimal edge covering



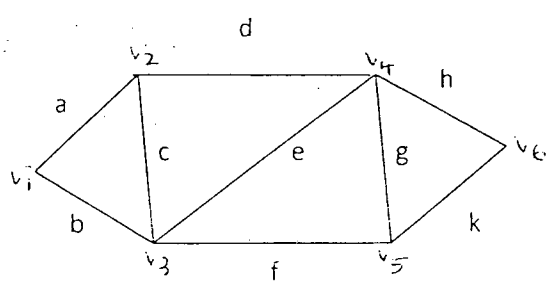
(OR)

13. b) (i) Sketch any one orientation of a complete graph of four vertices. Characterize the digraph in terms of binary relations. (8)

(ii) Find all the minimal dominating sets for the following graph using the method that uses Boolean arithmetic: (8)

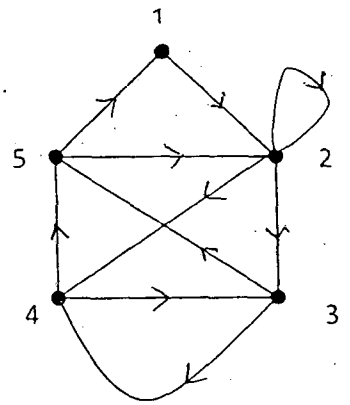


14. a) Use Paton's algorithm to find all the fundamental circuits in the following graph. Show the step-by-step procedure. (16)

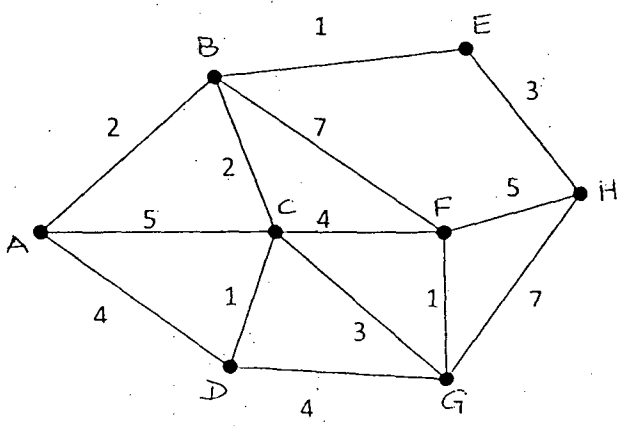


(OR)

14. b) Use Roberts and Flores' algorithm to find all the directed circuits in the following graph. Show the step-by-step procedure. (16)



15. a) Use Dijkstra's algorithm to find the shortest distance between the vertices A and H in the graph given below. Explain the step-by-step procedure. The distances between adjacent vertices is shown in the graph. (16)



(OR)

15. b) Explain the planarity testing algorithm proposed by Hopcroft and Tarjan. Discuss on the technique they have used to resolve ambiguity in adding paths. (16)