B.E./B.Tech.(Full Time) DEGREE END SEMESTER EXAMINATION, NOV/DEC 2012.

COMPUTER SCIENCE AND ENGINEERING BRANCH

SECOND SEMESTER (REGULATIONS 2008)

(2)

CS 9152 - DIGITAL PRINCIPLES AND SYSTEM DESIGN

Time: Three hours **Max. Mark : 100**

Answer ALL Questions.

PART A -(10 X 2 = 20 marks)

1. Given the two binary numbers X=1010100 and Y=1000011, perform the subtraction X—Y and Y—X by using 2's complements.
2. Draw the logic diagram for the following Boolean expression : F=XY+X'Y'+Y'Z
3. What are the differences between combinational and sequential circuits?
4. List the modules of HDL.
5. What is a Priority Encoder?
6. Compare SRAM vs DRAM.
7. Write the characteristic equations for T and JK flip flop.
8. Give the guidelines for state assignment.
9. What is Race condition and Cycle in asynchronous sequential network?
10. List the steps in merging a flow table.

PART –B (5 X 16 = 80 marks)

11. a) i) Simplify the following Boolean expression to A) Sum-of-product B) Product- of- sum using Karnaugh map (10)

F(A,B,C,D)= A'B'+ACD'+ABC+A'B'CD'+B'D

ii) Prove the following theorems:

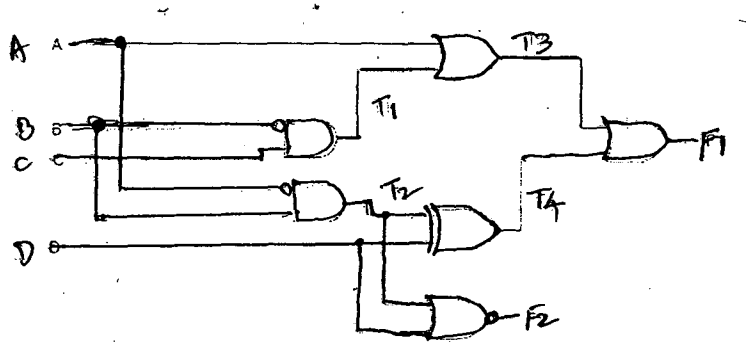
A. X+XY=X B. X+X=X C . X+1=1 (6)

12. a) i) With neat block diagram explain the BCD adder. (8)

ii) Analyze the following combinational circuit (8)

A. Derive the Boolean expressions for T1 through T4. Evaluate the outputs F1 and F2 as a function of the four inputs.

B. Draw the truth table for the circuit.



(OR)

b) i) A Majority circuit is a combinational circuit whose output is equal to 1 if the input variables have more 1's than 0's . The output is 0 otherwise. Design a 3-input majority circuit. (8)

ii) Design a 4-bit adder with carry look-ahead. (8)

13. a) i) Implement the following two Boolean functions with a PLA. (8)

$F(A,B,C)=\Sigma\ (0,1,3,4)$

$G(A,B,C)=\ \Sigma\ (0,5,6,7)$

ii) Write an HDL behavioral description of a 4-bit arithmetic logic unit. The circuit performs two arithmetic and two logic operations that are selected by a 2-bit input. The four operations are add, subtract, AND and OR. (8)

(OR)

b) i) Implement the following Boolean function with the multiplexer. (8)

$F(A,B,C,D)=\sum\ (0,2,5,7,8,11,14)$

ii) Design a 5 x 32 decoder by using 3 x 8 decoders and a 2 x 4 decoder. (8)

14. a) i) With neat diagram explain the 4 bit Universal Shift register. (6)

ii) A sequential circuit has two JK flip-flops A and B and one input x. The circuit is described by the following flip-flop input equations: (10)

$J_A=x \quad K_A=B'$

$J_B=x \quad K_B=A$

A. Derive the state equations A(t+1) and B(t+1)

B. Draw the state diagram of the circuit.

(OR)

b) i) Design a 3 bit counter using T flip flop (8)

ii) Reduce the state table and graph for the following state table. (8)

Present state	Next state		Present output	
	X=0	X=1	X=0	X=1
a	h	c	1	0
b	c	d	0	1
c	h	b	0	0
d	f	h	0	0
e	c	f	0	1
f	f	g	0	0
g	g	c	1	0
h	a	c	1	0

15. a) i) Discuss the hazards in combinational circuit. (8)

ii) Explain the procedure that must be followed to ensure a race-free state assignment. (8)

(OR)

b) An asynchronous sequential circuit has two internal states (Y_1 , Y_2) and one output (Z). The excitation and output functions describing the circuit are (16)

$Y_1 = X\,Y_1 + X'\,Y_2$

$Y_2 = X\,Y'_1 + X'\,Y_2$

$Z = Y_1$

A) Draw the logic diagram of the circuit

B. Derive the transition table and output map

C. Obtain the flow table for the circuit.