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UNIVERSITY DEPARTMENTS, ANNA UNIVERSITY – CHENNAI
B.E. DEGREE EXAMINATIONS, NOVEMBER 2012
R 2008, III SEMESTER

CS 9204 COMPUTER ARCHITECTURE

Time: Three Hours **Max. Marks: 100**

Answer All Questions

PART - A (10 X 2 = 20 Marks)

1. There are two options available to enhance the performance of a machine. One is to add a vector mode of computation that is 10 times faster than the normal mode of execution, which is used 70% of the time. Another is to double the clock frequency. Which of the two would be better?

2. Discuss the basic cell of an array multiplier.

3. Show how a stack can be implemented using the autoincrement / autodecrement addressing modes.

4. Identify the dependences in the following code snippet:
   ADD R1, R2, R3
   DIV R4, R1, R5
   ADD R5, R7, R4
   AND R5, R4, R2

5. What is a re-order buffer? How is it useful?

6. Consider a non-pipelined machine with 5 execution steps of lengths 50, 60, 75, 70 and 50 ns respectively. Suppose that due to overheads, pipelining the machine adds 4ns of overhead to each execution stage. Ignoring any latency impact, how much speedup in the instruction execution rate will we gain from the pipeline?

7. Show how a 16MB main memory can be realized using 64KB memory chips. Assume an interleaved memory organization with four banks.

8. A certain computer system has a 1GB main memory and 64KB cache memory organized using 4-way set associative mapping. Calculate the number of bits in each of the Tag, Set and Word fields of the memory address.

9. List down the functions to be performed by a serial I/O interface.

10. What is meant by program driven data transfer?

PART- B (5 x 16 = 80 Marks)

11. (i) Discuss the typical organization of a hardwired control unit.
For the single bus organization, write down the sequence of steps in order to do the following operation:
MUL (R1), R2,
where the format is Operation dst, src. (5+5)

(ii) Discuss the concept of nanoprogramming. What are its advantages and disadvantages? (6)

12. a. (i) Discuss the organization of a sequential binary multiplier. Simulate the multiplication algorithm for the numbers 8 and 10. (10)

(ii) Discuss the concept of a Booth's multiplier and a bit-pair recoded multiplier. (6)

OR

b. (i) Discuss the non-restoring division algorithm.
Simulate the same for the numbers 10 / 3. (10)

(ii) Discuss any six factors that need to be considered while designing the Instruction Set Architecture (ISA) of a processor. (6)

13. a. (i) Consider the following code and assume that the multiply instruction has a latency of 5, the divide instruction a latency of 10 and the add instruction a latency of 3. Also assume that there are separate functional units for effective address calculations, for ALU operations, and for branch condition evaluation. For a **speculative** processor, create a table showing when each instruction issues, executes, writes the result and commits, for one iteration of the loop and for atleast two instructions from the second iteration. Assume one CDB and that only one instruction can commit per clock cycle.
(10)

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loop:  LD      F0, 0(R1)
       ADDD    F0, F0, F2
       LD      F4, 0(R2)
       MULD    F0, F0, F4
       DIVD    F0, F0, F6
       SD      0(R2), F0
       DADDUI  R1, R1, #8
       DADDUI  R2, R2, #8
       DSGTUI  R3, R1, R2 (test if done)
       BNEZ    R3, loop
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(ii) What are multiple issue processors? Discuss briefly. (6)

OR

b. (i) Consider the code fragment given in question 13 a. Assuming a latency of 3 for MUL and DIV, and 2 for ADD, show the timing of this instruction sequence for the MIPS floating point pipeline without any forwarding hardware, but assuming a register read and a write in the same cycle "forwards" through the register file. Assume that the branch is handled by predicting it as not taken. If all memory references hit in the cache, how many cycles does one iteration of this loop take to execute? (10)

(ii) Discuss any three techniques that the compiler uses to exploit ILP. (6)

14. a. (i) Compare and contrast the various mapping policies used in cache memories. (6+4)
Consider a series of address references given - 2, 3, 11, 16, 21, 13, 64 and 48. Assuming a direct mapped cache with 8 one-word blocks that is initially empty, label each reference in the list as a hit or a miss and show the final contents of the cache.

(ii) Define Average Memory Access Time for a 2-level memory system. Discuss any four ways of reducing AMAT. (6)

OR

b. (i) Discuss the concept of virtual memory and show how a paged memory management technique is implemented. (10)

(ii) Discuss the basic cell of an associative memory and show how a 16 x 8 associative memory array is constructed. (6)

15. a. (i) Explain the interrupt driven mode of data transfer and the DMA driven data transfer, elaborating on how they are accomplished and their relative merits and demerits. (10)

(ii) Consider a computer system that has only one DMA request line, but has to service multiple devices requesting service. Discuss any two ways of handling this. (6)

OR

b. (i) What is the need for standard I/O interfaces?
Discuss in detail the PCI or USB interface. (10)

(ii) Compare and contrast memory-mapped I/O and I/O mapped I/O. (6)

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