Reg. No. .....

B.E / B.Tech. (Full Time) DEGREE END SEMESTER EXAMINATIONS, APR / MAY 2012
ELECTRONICS AND COMMUNICATION ENGINEERING
FOURTH SEMESTER

(3)

EC 281 DIGITAL ELECTRONICS AND SYSTEM DESIGN
(REGULATIONS 2004)

TIME: 3 hr Max Mark: 100

Answer ALL Questions

Part – A (10 x 2 = 20 Marks)

1. Convert the hexadecimal number F3A7C2 to binary and octal.
2. Simplify the Boolean functions $x(x+y)$ and $x'y'z + x'yz + xy'$ to a minimum number of literals.
3. Calculate the fan-out for the standard TTL gate for the following values of current $I_{OH} = 400\mu A$, $I_{IH} = 40\mu A$, $I_{OL} = 16mA$, $I_{IL} = 1.6mA$.
4. Define noise margin.
5. What is the role of priority encoder?
6. Mention the context of usage: ROM, EPROM and EEPROM.
7. State the significance of edge-triggered flipflop.
8. What are moore /mealy model?
9. Distinguish between stable and unstable state.
10. What is state table?

Part – B (5 x 16 = 80 Marks)

11. a. Find a circuit that has no static hazards and implements the Boolean function. (8)

$F(A,B,C,D) = \Sigma (0,2,6,7,8,10,12)$

11. b. Discuss the methods for designing race free and hazard free circuit with examples. (8)

12. a.i. Simplify the Boolean function F with don't care condition d in SOP & POS. (10)

$F(W,X,Y,Z) = \Sigma (0,1,2,3,7,8,10)$ & $d = \Sigma (5,6,11,15)$

ii. Implement the following function with NAND gates. (6)

$F(X,Y,Z) = \Sigma (0,6)$

(OR)

12. b.i. Draw the logic diagram corresponding to the following Boolean expression (8)

without simplifying them. (A+B)(C+D)(A'+B+D) & (AB+A'B') (CD'+C'D)

ii. Determine the prime implicants of the function F(w,x,y,z) (8)

$F(w,x,y,z) = \Sigma (1,4,6,7,8,9,10,11,15)$

13. a. With neat sketches describe the operation of TTL and HTL. (16)

(OR)

13.b. Explain the working principle of NMOS and CMOS logic gates with necessary diagrams. (16)

14. a.i. A combinational circuit is defined by the functions, (8)

$F_1(x,y,z) = \Sigma\, m(1,2,4,6)$, $F_2(x,y,z) = \Sigma\, m(0,1,6,7)$

$F_3(x,y,z) = \Sigma\, m(2,6)$

Implement the circuit with PLA.

ii. Construct a 3 to 8 decoder using two 2 to 4 decoder. (4)

iii. Implement a full-adder with two 4X1 multiplexer. (4)

(OR)

14. b.i. Implement the following boolean function with an 8X1multiplexer. (8)

$F(A,B,C,D) = \Sigma\, (0,3,5,6,8,9,14,15)$

ii. With a example discuss about PAL and PLA circuit design. (8)

15.a. i. Design a synchronous BCD counter with JK flip-flops. (10)

ii. Write short notes on semiconductor memories. (6)

(OR)

15.b. i. A sequential circuit has two D flip-flops, one input X and one output Y. The flip-flop input functions and the circuit output function are as follows $DA(A,B,X) = \Sigma(2,4,5,6)$ $DB(A,B,X) = \Sigma(1,3,5,6)$, $Y(A,B,X) = \Sigma(1,5)$. Obtain the state equations, state table, state diagram and logic diagram. (12)

ii. State the significance of triggering of flip-flop. (4)