(48)

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B.E. (Full-time) DEGREE End Semester EXAMINATIONS, April / May 2011

ELECTRICAL & ELECTRONICS ENGINEERING,

Seventh Semester – (Regulation 2004)

EE 471 - Digital Signal Processors

Time : 3 hr Answer ALL questions Max. marks : 100.

PART – A (10 x 2 = 20)

1. What is a single-pole recursive high pass filter?
2. Distinguish between a Braun's multiplier and a Baugh – Wooley multiplier.
3. Draw the hardware block diagram of a barrel shifter, capable of performing left shift of a given 4-bit unsigned number.
4. What are the computational savings in evaluation of DFT using radix-2 FFT algorithms?
5. State the advantages of floating point representation?
6. Why is it necessary to provide 'guard bits' in the accumulator?
7. Comment on the location of zeros of anyone type of FIR filter?
8. What do you understand by 'In-place Computation'?
9. Why is it necessary to clear CNF bit (by employing 'CLRC CNF' instruction), before parameter updating segment of adaptive FIR implementation on TMS2x DSPr?
10. What is h[n] of an ideal (zero phase) Low Pass Filter?

PART – B (5 x 16 = 80)

11. Discuss the architecture and features of anyone fixed point or floating point Digital Signal processor chip. Also discuss the operation of any two of its instructions.

12. a) i) "s-to-z mapping based on backward difference method, maps the $j\Omega$ axis onto a circle of radius ½ centered at (½ ,0) – Prove this statement. (6)

ii) By means of DFT and IDFT, determine the sequence x(n) corresponding to the circular convolution of the sequences $x_1(n)$ and $x_2(n)$ given by,

$x_1(n) = \{ 0\ 3\ 2\ 1\}$, and $x_2(n) = \{ 1\ 2\ 3\ 0 \}$. Also verify your answer by directly performing the circular convolution. (10)

OR

OR

b) i) Find the 6-point DFT of x[n]=(0 1 2 3 2 1), by finding the z-transformation and suitably substituting values for z. (7)

ii) Find the 8-point DFT of x[n]=(1 2 3 3 2 1 0 0), by employing butterfly structure and DIT. Also verify your answer by any other method. (9)

13. a) i) Design a digital Butterworth low pass filter that satisfies the constraints: $0.7 < |H(e^{jw})| < 1$, for $0 < w < \pi/4$, and $|H(e^{jw})| < 0.3$, for $\pi/2 < w < \pi$. Use bilinear transformation and assume T = 1 sec. (8)

ii) Write a program for generating Pseudo Random Bit Sequence. You may use the fixed point Digital Signal processor TMS320C2407 or floating point Digital Signal processor TMS320C30. Add comments to your program, briefly explaining the algorithm employed. (8)

OR

b) i)Discuss the methodology for FIR filter design using 'windowed sinc filter'. Also distinguish between Hamming and Hanning windows. (6)

ii) Write down the program for IIR filter using the floating point Digital Signal processor TMS320C30 and discuss the working principle of the program. (10)

14. a) i) What is 'bit reversed addressing' mode? (3)

ii) How is 'circular buffer' useful? (4)

iii) Write a MATLAB program for rearranging the elements of a given vector in bit reversed sequence, after performing zero-padding to make the vector size equal to the next higher 2^n. (9)

OR

b) i) Along with a block diagram of the event manager A of TMS320C2407, discuss its features. Write a program for generating a square waveform. (8)

ii) Explain how convolution sum can be computed using the instruction MAC by writing a program. What is the extra operation performed by MACD instruction when compared to MAC instruction?How is this used in real-time applications?(8)

15. a) What is an adaptive filter? Discuss the basics of Least Mean Square algorithm for filter parameter adaptation. Write a program for implementing an adaptive FIR filter on the fixed point Digital Signal Processor TMS 320C2407, employing Least Mean Square algorithm.

OR

b) Write down the difference equation defining Fibonacci series. Employing unilateral Z-transform technique, solve it and obtain a generic expression for the n^{th} element of Fibonacci series. Also write a program in TMS320C30 for generating the first ten elements of the Fibonacci series, based on its definition.