B.E (Full Time) DEGREE END SEMESTER EXAMINATIONS, APRIL/ MAY-2011
ELECTRICAL & ELECTRONICS ENGINEERING BRANCH
CEG, ANNA UNIVERSITY CHENNAI
EIGHTH SEMESTER (VIII)
EE518- VLSI DESIGN

Time: 3 Hrs Max.Marks: 100

Answer ALL Questions

Part -A (10 x 2=20 Mark)

1. What is stick diagram? State its advantages.
2. State the significance of Lamda based rules.
3. Draw the layout diagram for an inverter.
4. List the Applications of Tally circuits.
5. Draw the CMOS structure for a not gate.
6. Compare CPLD and FPGA programmable logic devices.
7. How many logic elements are required to implement an 16:1 multiplexer using XC9500 series device.
8. Draw the Macrocell architecture of PAL16R8 and state its significances.
9. Write the behavioral VHDL code for a half adder.
10. Write a VHDL code for a tri-state inverter.

Part-B (5 x 16=80 Mark)

11. Explain the various steps involved in fabrication of ICs using NMOS Processing Technique.

12. a) Design a Digital BiCMOS circuit that implements the function f = a.b.c + c.d.e

[Or]

b) Derive the current equation of MOS device and discuss the transfer characteristics, output characteristics, Pull up –Pull down ratios, timing and Fan-out consideration of CMOS inverter.

13. a) Draw the circuit diagram for a dynamic logic gate that has an output of f = a.(b+c+d), using the smallest number of transistors.

[Or]

b) Design a Full Adder using
(i) CMOS switches.
(ii) CMOS transmission gates.
Assess the efficiency of each implementation by counting the no of switches used. Which is more efficient? Why?

14. a) Explain the features of MAX 7000 device with its architecture.

[Or]

b) With neat diagrams explain the CLB, Switch matrix and IOB of XC4000 device.

15. a) Write the behavioral and structural VHDL code for a 3:8 decoder.

[Or]

b) Write a structural VHDL code for an 8 bit Full Adder.