B.E. / B.Tech DEGREE END SEMESTER EXAMINATIONS, NOV / DEC 2013

ELECTRONICS AND COMMUNICATION ENGINEERING BRANCH

SECOND SEMESTER

EC 181 – ELECTRONIC DEVICES

(REGULATIONS 2004)

Time: 3 Hours Max.Marks:100

Answer All Questions

Part-A (10 x 2 = 20 marks)

1) Compute the conductivity of a silicon semiconductor which is doped with acceptor impurity to a density of 10^{22} atoms / m^3. Given that $n_i = 1.4x10^{16}$ /m^3. $\mu_n = 0.145$ m^2 / V-s and $\mu_p = 0.05$ m^2 / V-s
2) Sketch the conduction and valence bands before and after diffusion of carriers in a PN junction.
3) Distinguish between avalanche and Zener mechanisms.
4) Mention the applications of Schottky barrier diode.
5) In a common base connection, the emitter current is 6.28mA and the collector current is 6.20mA. Determine the common-base d.c current gain.
6) Define thermal runaway.
7) Compare JFET and MOSFET.
8) Why low power FET is called as square law device?
9) What is the use of heat sink in power transistors?
10) Draw the two transistor analogy of an SCR.

Answer All Questions

Part-B (5 x 16 = 80 marks)

11. (i) Derive the conductivity equation for an N-type and P-type semiconductor (8)

(ii) Define Hall effect and Explain its applications. (8)

12. (a) Explain the action of PN Junction diode under forward and reverse bias with its VI Characteristics (16)

(or)

(b)(i) Define the following terms:

Diffusion resistance

PIV

Maximum power rating (6)

(ii) Explain how metal semiconductor junction act as ohmic contact (10)

13. (a) (i) Explain how transistor acts as amplifier (8)

(ii) Draw the a.c equivalent circuit of CC amplifier using h-parameter model and derive the equations for input and output impedance. (8)

(or)

(b) (i) Draw the Ebers-Moll model for a PNP transistor and give the equations for emitter and collector current. (10)

(ii) Construct fixed bias circuit and derive its stability factor (6)

14. (a) Explain qualitatively the shapes of I_D versus V_{DS} and I_D versus V_{GS} characteristics for three types of FET's (16)

(or)

(b) (i) Briefly explain the effects of channel length modulation in MOSFET (8)

(ii) Calculate the operating point of the self biased JFET having V_{DD}= 20V,maximum value of drain current is 10 mA and V_{gs} = -3V at I_D =4mA. Also determine the values of R_D and R_S to obtain this bias condition. (8)

15. (a) Describe in detail with neat diagram, the construction and operational details of Uni Junction transistor (16)

(or)

(b) Explain the working principle of DIAC and TRIAC in detail (16)