(6)

BE/BTECH (FULL-TIME) DEGREE END SEMESTER EXAMINATIONS NOV/DEC-2013
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
III SEMESTER
EC8301 ELECTRONIC CIRCUITS-I
(Regulation 2012)

Time:3Hrs **Max Marks:100**

Answer all questions
Part-A (10 X 2=20 Marks)

1) What are the design constraints required for thermally stabilized biasing circuit.
2) What is the role of bypass capacitor in BJT CE-amplifier circuit?
3) Determine the input impedance of common base amplifier.
4) A small signal source $Vi(t)=20\cos 20t+30\sin 10^6 t$ is applied to a transistor amplifier as shown in Figure-1. The transistor has $\beta=150$, $ro=\infty$ and $r_\pi=3k\Omega$. Determine Vo(t)?
5) Find the unity gain bandwidth of MOSFET whose $g_m=6mA/V$, $C_{gs}=8pF$, $C_{gd}=4pF$ and $C_{ds}=1pF$.
6) The ac schematic of an NMOS common-source stage is shown in the Figure-2, where part of the biasing circuits has been omitted for simplicity. For the N-channel MOSFET M1, the transconductance, gm =1mA/V, and body effect and channel length modulation effect are to be neglected. Find the lower cutoff frequency?
7) Draw the small signal equivalent circuit diagram of PMOS and NMOS transistor by considering body effects.
8) The small-signal resistance (i.e.,dV_B/dI_D) in kΩ offered by the n-channel MOSFET M2 shown in the Figure-3, at a bias point of $V_B=2V$ is (device data for M2: device Transconductance parameter $K_N=\mu_n Cox(W/L)=60\mu A/V^2$, threshold voltage Vtn=1V, and neglect body effect and channel length modulation effects).
9) The DC-load line of MOSFET-Common Source amplifier is shown in Figure-4, Let $V_{DSsatmin}=0.3V$, $R_D=R_L=2.5K$. Determine its maximum output voltage swing?
10) Determine the output impedance of a JFET amplifier shown in Figure-5. Let gm=2mA/V and $\lambda=0$.

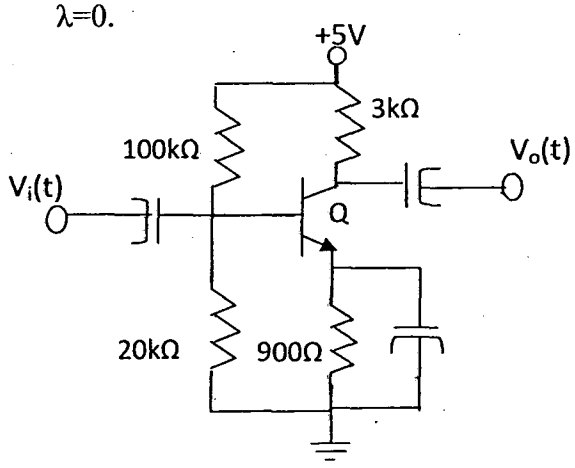

Figure-1

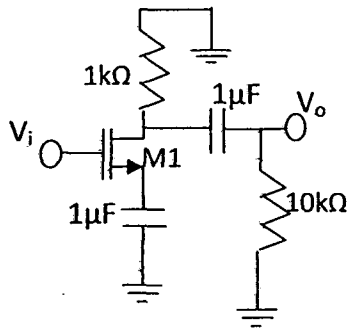

Figure-2

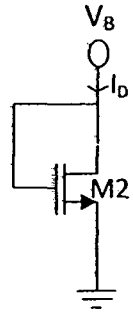

Figure-3

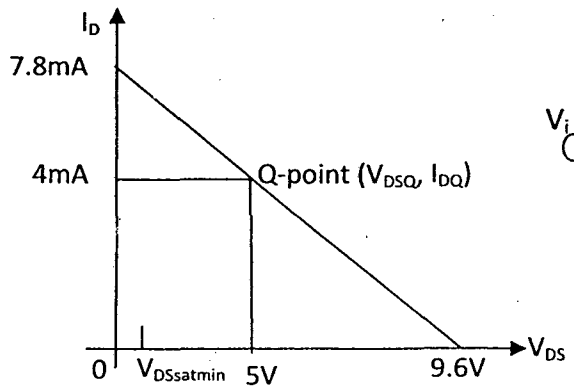

Figure-4

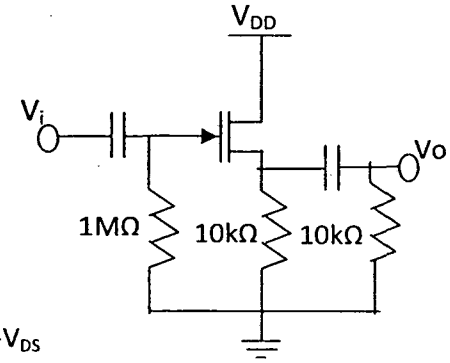

Figure-5

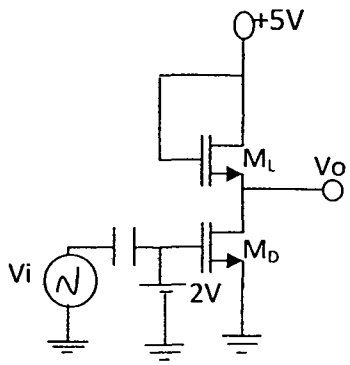

Figure-6

PART-B (5X 16=80 Marks)

11) i)With neat circuit diagram explain CMOS differential amplifier with active load. Draw its equivalent circuit and derive for its CMRR using small signal parameters. (12)

ii) For the NMOS inverter circuit with saturated load (vide Figure-6), the transistor parameters are: (device data for M_D: Vtn_D =1V, $Kn_D=\mu_n Cox(W/L)=100\mu A/V^2$, $\lambda n_D=0$ and device data for M_L: Vtn_L =1V $Kn_L=\mu_n Cox(W/L)=20\mu A/V^2$, and $\lambda n_{L=}$ 0). Draw its voltage-transfer characteristics curve, and mark down its transition points. (4)

12)a)i)Define and derive the stability factors for BJT self bias (voltage-divider bias) circuit. (10)

ii) Design a JFET circuit with self bias to operate as amplifier with I_D = 2mA, I_{DSS} = 12mA and V_P = 4V. Assume V_{DD} = 22V, also calculate the maximum peak to peak output voltage of your designed circuit. (6)

(OR)

b) i) The parameters for each transistor in the circuit in Figure-7, are β =100, and V_{BEon}=0.7V. Determine the Q-point values of base, collector and emitter currents in Q_1 and Q_2. **(please note that β=hfe)** (8)

ii) Determine the change in collector current produced in each bias referred to in example Figures 8(a) & 8(b). When the circuit temperature raised from 25°C to 105°C and I_{CBO} =15nA @ 25°C. (8)

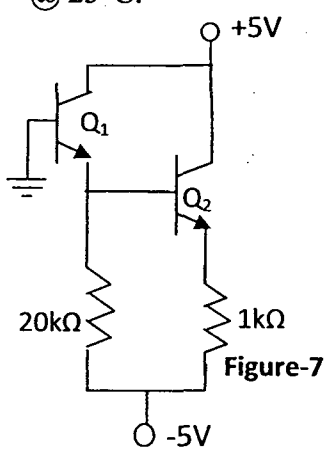

Figure-7

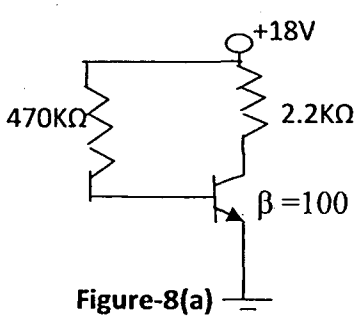

Figure-8(a)

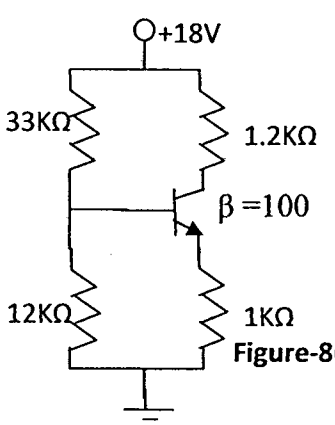

Figure-8(b)

13)a)i) For the circuit shown in Figure-9, the transistor parameters are β=125, V_A=∞, V_{CC}=18V, R_L=4kΩ,R_E=3kΩ, R_C=4kΩ, R_1=25.6kΩ and R_2=10.4kΩ. The input signal is a current. Determine its small signal voltage gain, current gain, maximum voltage gain and input impedance. (12)

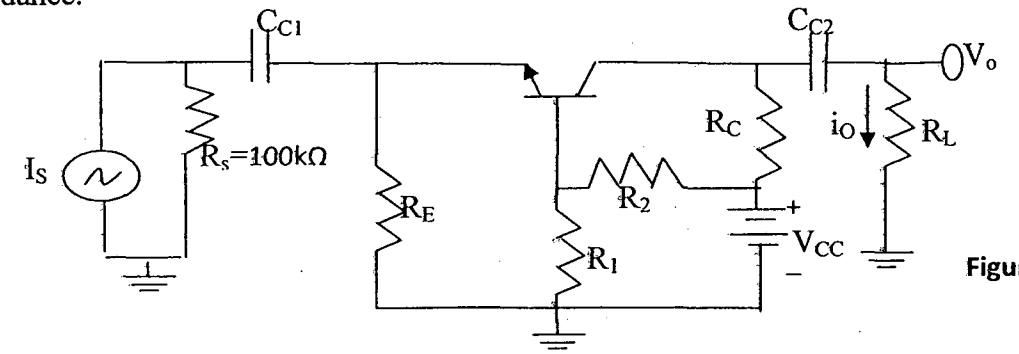

Figure-9

ii) Derive for current gain of Common Emitter amplifier (self-bias) circuit. (4)

(OR)

b)i) A differential amplifier has a differential gain of 70 dB and CMRR of 90 dB, if V_1 = 20μV and V_2 = 16μV.calculate the output voltage of amplifier and common mode gain. (4)

ii) Draw the circuit diagram of bootstrapped emitter follower with its equivalent circuit, derive for its input and output impedance. (6)

iii) Draw a cascode amplifier, with the help of its equivalent circuit diagram derive its voltage-gain and input impedance. (6)

14)a)i) Draw a NMOS discrete common gate amplifier and its equivalent circuit. Derive for its A_V, R_{in} and R_0. (10)

ii) For the p-channel JFET common-source amplifier in Figure-10, the transistor parameters I_{DSS}=8mA, V_P= 4V and λ=0. Design the circuit such that I_{DQ}=4mA, V_{SDQ}=7.5V, A_V= -3 and R_1+R_2=400kΩ. (6)

(OR)

b)i) Determine voltage gain, current gain, input impedance and output impedance of JFET source follower amplifier. (10)

ii) Determine the value of R_D, R_S, voltage gain, input and output impedance of the amplifier having parameters I_D = 0.5mA Vtp=1.2V, K_P'=μ_PCox=80μA/V^2 , V_{SD}=4V and (W/L)= 6.25 (vide Figure-11) (6)

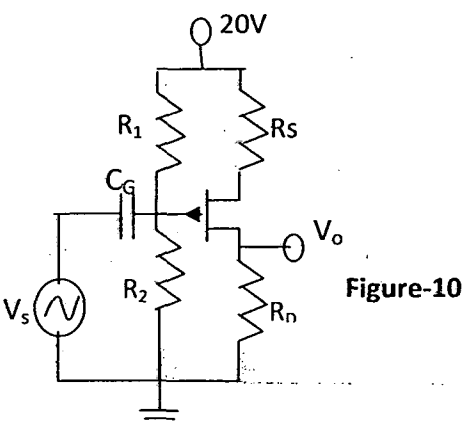

Figure-10

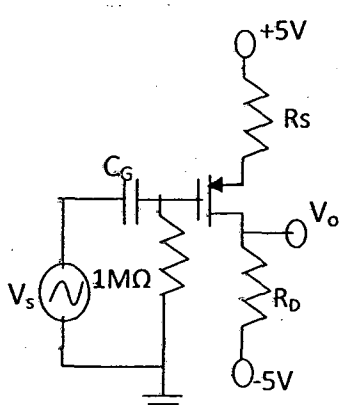

Figure-11

15)a)i) Derive for fβ and fα. (6)

ii) For the circuit shown in Figure-12 has following parameters: h_{fe} =125, C_π = 24pF , C_μ = 3pF, wiring capacitance is 8pF. (x) Determine its mid-band gain, upper-cut off frequency (y) Find the value of C_{C1}, C_{C2} and C_E by assuming lower cut-off frequency of 100 Hz. (10)

(OR)

b) For the circuit shown in Figure-13, the NMOS transistor parameters are: $Kn=\mu_n Cox(W/L)$ $=2mA/V^2$, V_{GSQ}=3.25V, Vtn=2V, λ=0, C_{gd}=0.1pF and C_{gs}=1pF. Assume $C_G=C_D=C_S$ =1pF. Calculate the mid-band gain, input impedance, output impedance, bandwidth and Maximum output voltage swing. (16)

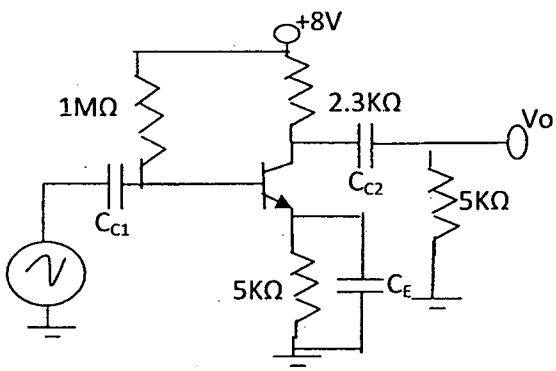

Figure-12

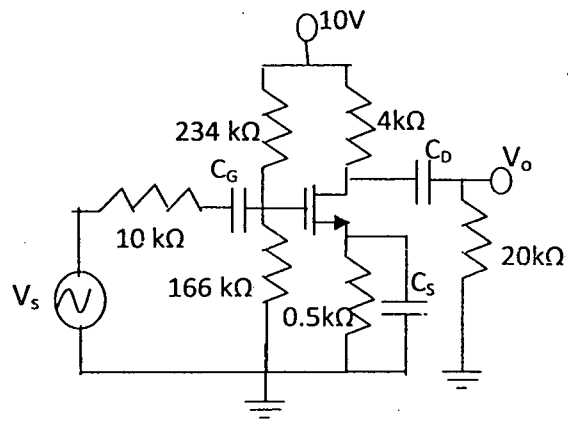

Figure-13