9/12/13

(7)

BE (Fulltime) Degree End Semester Examinations, Nov/Dec 2013
Department of Electronics and Communication Engineering
III Semester
EC272 Electronic Circuits I
Reg-2004

Total Marks:100

PART-A (10 X 2 =20 Marks)

1) Compare CE, CB and CC amplifiers.
2) Define CMRR of BJT amplifier. How to improve it?
3) Draw the small signal model of Common-Gate amplifier.
4) Compare NMOS inverter with resistive, Enhancement, depletion loads.
5) Draw the high-frequency model of BJT transistor.
6) Define Miller effect.
7) List-out the advantages of Power MOSFETs over Power BJTs.
8) What is meant by cross-over-distortion? How to overcome it?
9) Differentiate between FWR and bridge rectifier.
10) Compare between LC and π filter.

PART-B (5 X 16 =80 Marks)

11)a)i) Determine mid-band gain and upper cut-off frequency of Common Emitter amplifier (8)
ii) Determine mid-band gain and upper cut-off frequency of Common Source amplifier (8)

12)a) Explain the DC characteristics of a CMOS inverter with necessary diagrams and derivations. (16)

(OR)

b) i) For each transistor in the Darlington circuit shown in Figure 1 has the parameters of β=100, V_A=∞. Determine its overall voltage gain, input impedance and output impedance (8)

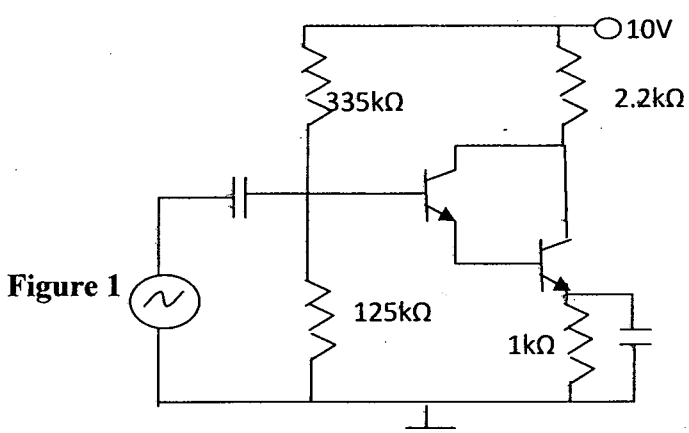

Figure 1

(ii) Determine the small signal voltage gain, input impedance and output impedance of common source FET amplifier (8)

13a)i) Determine Mid-band gain, input impedance and output impedance of Common-drain amplifier. (8)

ii) Determine mid-band gain, input impedance and output impedance of NMOS inverter with Depletion mode load. (8)

(OR)

b(i) For the circuit shown in Figure 2, let $V_{DD}=V_{SS}=1.5V$, Vtn=0.6V, Vtp=-0.6V, all channel lengths=1μm, $Kn=200\mu A/V^2$, $Kp=80\mu A/V^2$ and $\lambda=0$. For Iref=10 μA, Find the widths of all transistors to obtain $I_2=60\mu A$, $I_3=20\mu A$ and $I_5=80\mu A$. It is further required that the voltage at the drain of Q2 be allowed to go down within 0.2V of the negative supply and voltage at the drain of Q5 be allowed to go up to within 0.2V of the positive supply. (10)

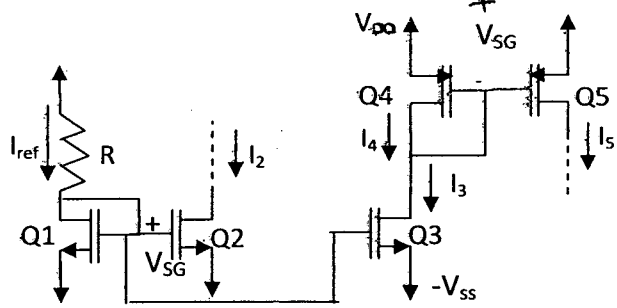

Figure-2

ii) Determine the mid-band gain, input-impedance and output impedance of CMOS common-source amplifier. (6)

14)a)i)Derive an expression to show the power efficiency of Class C power amplifier. (8)

ii) Explain in detail of Class S large signal amplifier. (8)

(OR)

b)i) Calculate the actual efficiency of the Class A output stage. Consider the common-source circuit in Figure 3. The circuit parameters are $V_{DD}=10V$, $R_D=5k\Omega$, $\beta n=2mA/V^2$, Vtn=1V and $\lambda=0$. Assume the output voltage swing is limited to the range between the transition point and $V_{DS}=9V$ to minimize the nonlinear distortion (8)

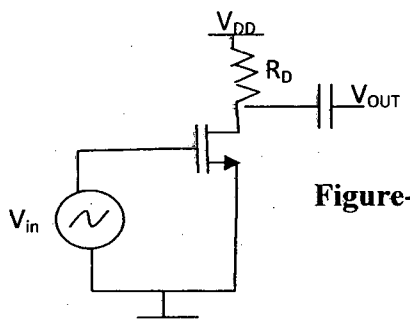

Figure-3

ii) Explain in detail of Class-AB power amplifier with darlington output stage (8)

15)a) Explain the Switched-Mode power supply design in detail (16)

(OR)

b)i) Explain the AC power control using SCR in detail (8)

ii) Explain the performances measures of rectifiers in detail (8)