21/11/13.

(24)

Reg. No. .....

B.E/B.TECH(FT) END SEMESTER EXAMINATIONS NOV/DEC 2013
ELECTRONICS & COMMUNICATION ENGINEERING
SUBJECT : EC8351 - DIGITAL ELECTRONICS AND SYSTEM DESIGN
R-2012

Duration : 3 Hours **Max Marks: 100**

PART A (10 x 2 = 20)

1. Represent the unsigned decimal number 8723 into its equivalent BCD.
2. For the output F to be 1 in the logic circuit shown, What should be the input combination?.

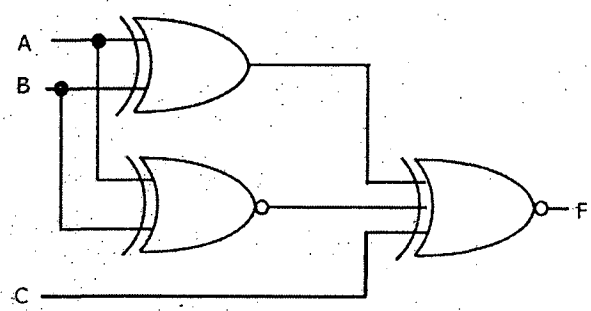

Fig. 1

3. A combinational circuit is specified by the Boolean expression f(A,B,C) = ∑(2,3,5,6,7). Implement the circuit with decoder.
4. Draw the PLA circuit to implement the function F = (A'B + AC' + A'BC').
5. Derive the characteristic equation of SR flipflop?.
6. Compare Moore and Mealy Circuits.
7. Define critical and non critical race?.
8. What are the assumptions that must be made for fundamental mode circuits?
9. Define fan in and fan out.
10. What is dynamic memory?.

PART - B (5 x 16 = 80)

11. i. Using Tabulation method simplify the Boolean function
F(w,x,y,z) = ∑(2,3,4,6,7,11,12,13,14) which has the don't conditions d(1,5,15). (12)

ii. Identify the gate realised at Z and write the Boolean Expression which gives the relationship between P, Q, R and M1? (4)

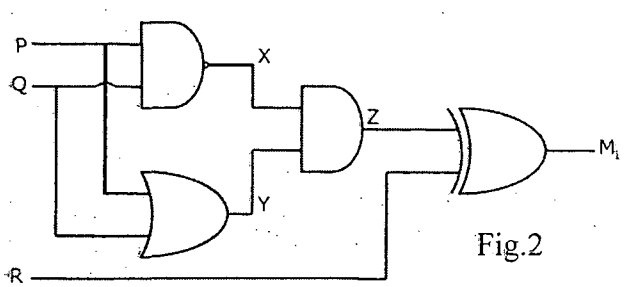

Fig.2

12. a. i. Design a BCD to seven segment decoder that accepts a decimal digit in BCD and generates the appropriate output for segments in display indicator. (12)

ii. Consider the half adder circuit which takes two binary inputs and generates Sum and Carry. Implement the half adder circuit with NOR gates only. (4)

(OR)

b. i Design an octal to binary encoder. (6)

ii. Implement a BCD to gray code converter using ROM architecture. (10)

13. a. i. A clock sequential circuit with single input x and single output z produces an output z = 1 whenever the input x completes the sequence 1011 and overlapping is allowed. Obtain the state diagram, minimize the state table and design the circuit with D flip flops. (12)

ii. Will the given circuit result in race around problem? Justify. (4)

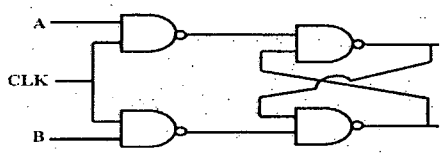

Fig.3

(OR)

b.i. What are the counting sequences (Q1, Q2) for the counter shown in the figure. The initial sequence is (0,0). (4)

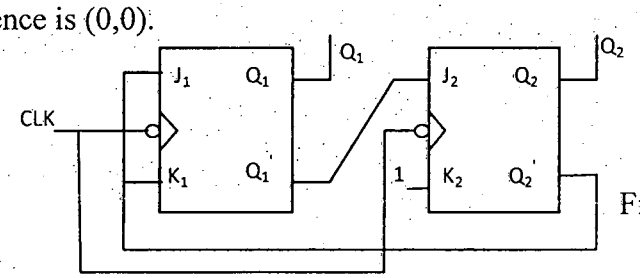

Fig.4

ii. Design a synchronous counter using J-K Flip-Flops to count the following sequences.
0010, 0011, 1010, 1000, 1100, 0001 and repeats. (12)

14. a. i. Design a gated latch circuit with two inputs G(gate) and D (data) and one output Q. Binary information present at the D input is transferred to the Q output when G is equal to 1. The Q output will follow the D input as long as G = 1. When goes to 0, the information that was present at the D input at the time the transition occurred is retained at the Q output. The gated latch is a memory element that accepts the value of D when G = 1 and retains this value after G goes to 0. Once G = 0, a change in D does not change the value of the output Q. (12)

ii. With an example discuss hazards in combinational circuits. (4)

(OR)

b. i. Consider a circuit with two inputs (x_1 and x_2) and one output (Z). The output is 1 only when x_1 and x_2 are 1 with x_1 going 1 first. (12)

ii. Write notes on cycles in asynchronous circuits. (4)

15. a. i. With the help of a neat diagram, explain the working of a two-input TTL NAND gate. (10)

ii. Explain the working principle of 6T based SRAM cell. (6)

(OR)

b. i. With the help of neat diagram explain the working of a two input CMOS NAND gate. (10)

ii. Write notes on the merits and demerits of various logic families. (6)