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(27)

Dept. of ECE, CEG Campus, Anna University
End Semester Examination Nov 2013 B.E(ECE) VII Semester (FT)
EC 9076 CMOS Analog IC Design II – Functional Blocks
Answer All Questions
Part A (10x2=20 Marks)

Q1. In block diagram shown in shown in Fig.1, consider a single tone output of frequency fs/10 that needs to be generated. With the help of spectral plots, explain the function of the analog hold and reconstruction filters.
Q2. When the same sinusoidal signal is sampled, it gives two different spectra as shown Fig. 2a and Fig.2b. Qualitatively explain how this difference in spectra can come about.
Q3. Fig.3 shows the diagram of segmented current steering DAC. Indicate the LSB and MSB values of the currents and state totally how many bit DAC this system represents.
Q4. Explain why the commonly used term 'bottom gate sampling' may not be technically correct.
Q5. In the context of Sample and Hold circuits, explain which particular problem is addressed by bootstrapping.
Q6. Explain how higher OSR can help in relaxing the design complexity of the antialias filter.
Q7. A 12 bit ADC will typically have an ENOB less than 12 bits. Why should it be so.
Q8. What are the factors that determine the size of the hold capacitor in a sample and hold circuit.
Q9. Draw the transistor level diagram of any one comparator circuit that will regenerate the difference between two inputs V+ and V-
Q10. Suppose glitches can be tolerated in a given application, what architecture of DAC would you prefer to use and why.

Part B(16x5=80 Marks)

Q11. (i) Consider the circuit shown in Fig.4. Assume that each input can vary from 0 to 2.5V. What is the peak to peak differential voltage. What is the LSB value for this case (i.e specify Δ value for this case). Assuming a uniformly distributed input which spans the full differential input range, what will be the variance of quantization noise for this case. What will be variance of thermal noise due to the sample and hold circuit.

(ii) Consider Fig.5a. What is the problem of hold mode feedthrough in this case. Reducing R_{on} in the figure is suggested as one possible way of reducing hold mode feedthrough. Another possible solution is to use the circuit shown Fig.5b. Explain how each of these schemes can help reduce the hold mode feedthrough problem.

Q12.a. (i) Consider Fig.6. The output voltage after T_{off} can be represented as $V_{out} = V_{in}(1+\varepsilon) + V_{os}$. Assuming fast gating, and that the gate voltage changes from ϕ_h to zero, determine the expressions for Vos and ε.

(ii) Consider Fig.7. In the signal paths of V^+ and V^-, there are three NMOS transistors in each path. Explain the function of each of these three NMOS transistors.

(iii) Consider Fig.8. Explain how the problem of charge injection is reduced by bottom gate sampling in this circuit. Express Vout as $V_{in}(1+\varepsilon) + V_{os}$ and determine the expressions for Vos and ε. What can you say about the charge injection due to the transistors M2 and M3.

OR

Q12.b Consider Fig.9a which shows the equivalent circuit Sample and Hold circuitfollowed by a switched capacitor amplifier during the track phase and hold phase. First determine the equivalent output impedance of the switched capacitor amplifier in Fig.9b. Then determine the total integrated output noise voltage due to both the hold phase and the track phase.

Q13a. (i) Two identical transconductors are connected to form a regenerative comparator. Assume that the transconductance of each is Gm and that the load on either side a capacitance C. Give the expression for the comparator gain as a function of resolution time τ_D.

(ii) Assuming a power supply of V_{DD} how do you define metastability condition.

(iii) Assume an amplifier of gain Av is to be used for the comparators in a B bit flash ADC output to vary between the supply rails between V_{DD} and 0 and the full scale input to be denoted by V_{FS}. Assuming that the pdf of the input is uniform, and a resolution time of τ_D determine an expression for probability of metastability.

OR

Q13.b (i)The diagram shown in the Fig.10 shown is to be used for offset cancellation of the op-amp. Sketch the appropriate waveforms for ϕ_1 and ϕ_2 and determine the expression relating the output voltage, input voltage and the offset voltage. Is the input voltage to output voltage amplification taking place under open loop condition without feedback or is it with negative feedback.

(ii) Suppose the same diagram in Fig.10 is to amplify the voltage difference between Vin and Vref, how would you modify the circuit. Further, suppose Vin and Vref are each available as differential voltages, how would your circuit get modified.

Q14.a. Consider the pipeline ADC scheme shown in Fig.11 Using gain, summing/defference, ADC and DAC blocks, indicate a possible realization for the stages 1,2 and 3. Give the possible expression for the Dout in terms of D1, D2, D3.

OR

Q14.b Consider the diagram in Fig.12 Explain the switching sequence, the relationship between capacitor values and the operation of a 5 bit SAR ADC using this diagram.

Q15.a For the sigma delta converter shown in Fig.13, determine a relationship between OSR, bit resolution B and the SQNR (dB)

OR

Q15.b (i)Determine STF and NTF for the structure shown in Fig.14

(ii) Consider the circuit shown in Fig.15. Obtain a relationship to express $V_0(n)$ in terms of $V_i(n)$. How can this circuit be modified to obtain a single bit sigma delta modulator.

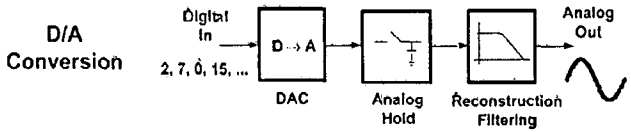


Fig.1

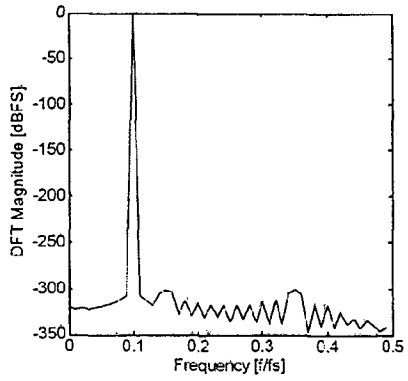


Fig.2a

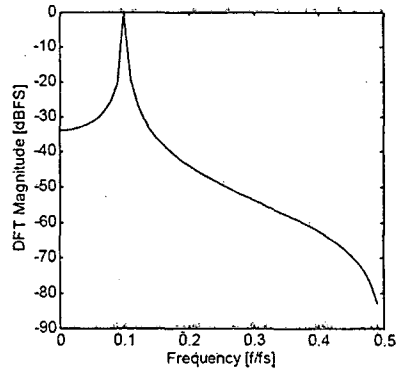


Fig.2b

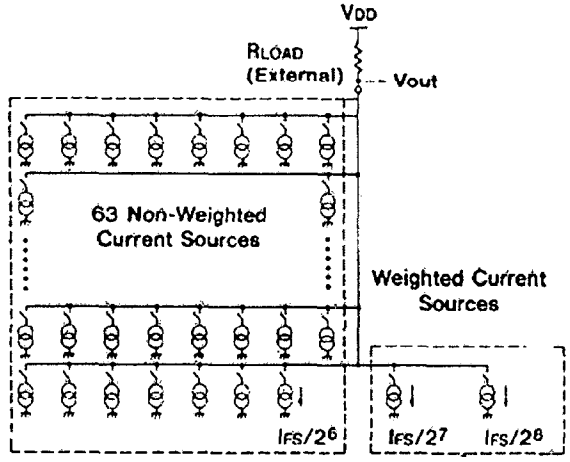


Fig.3.

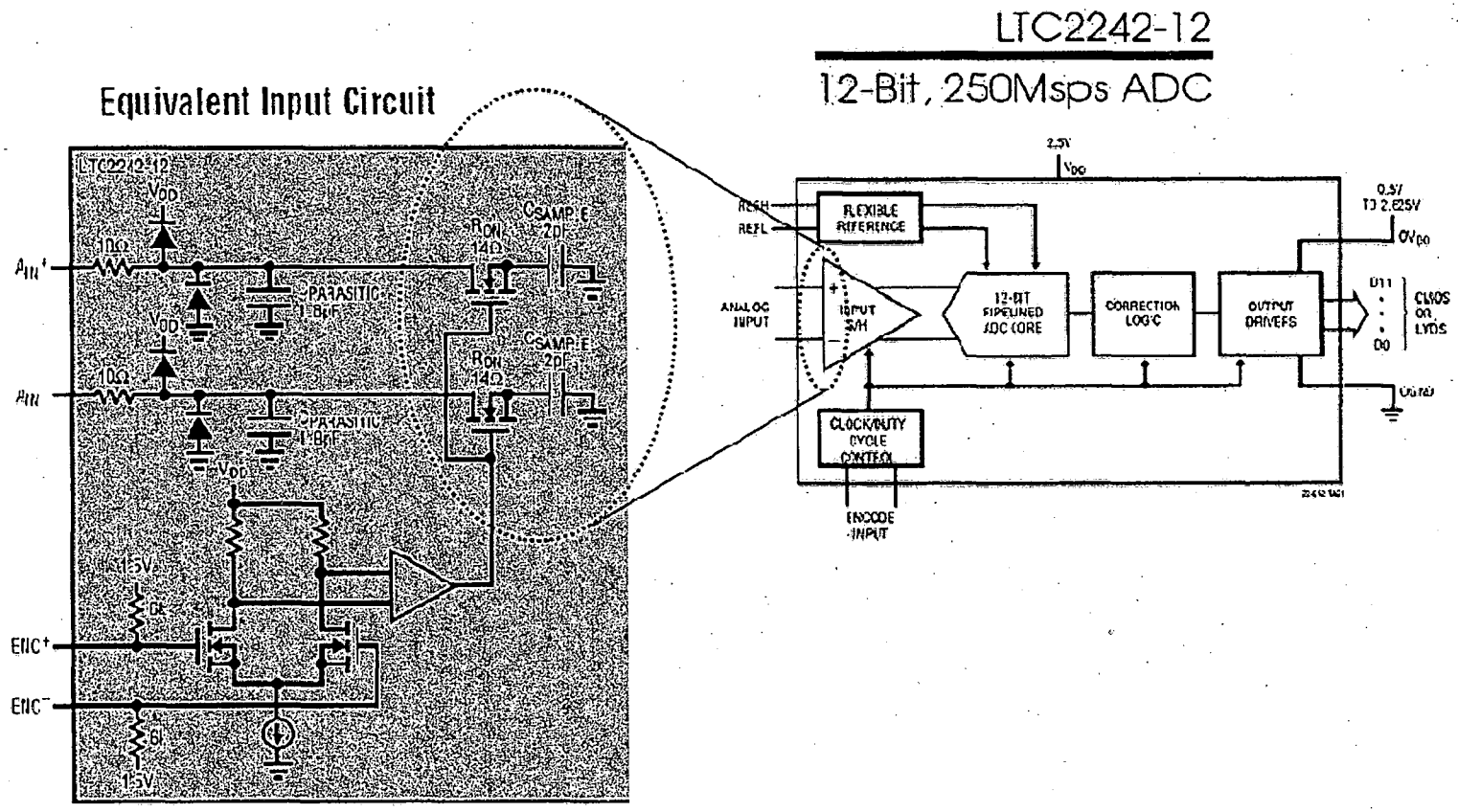

LTC2242-12
12-Bit, 250Msps ADC
Equivalent Input Circuit
LTC2242-12
VDD
10Ω
AIN+
AIN–
PARASITIC 1.8pF
RON 14Ω
CSAMPLE 2pF
ENC+
ENC–
1.5V
6k
FLEXIBLE REFERENCE
REFH
REFL
ANALOG INPUT
INPUT S/H
12-BIT PIPELINED ADC CORE
CORRECTION LOGIC
OUTPUT DRIVERS
CLOCK/DUTY CYCLE CONTROL
ENCODE INPUT
CMOS OR LVDS

Fig.4

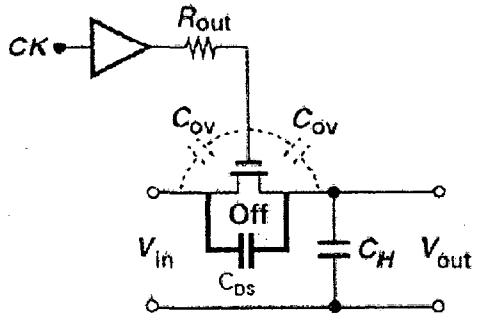


Fig.5a

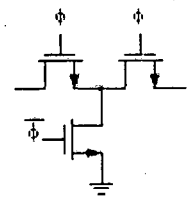


Fig.5b

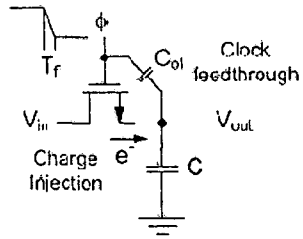


Fig.6

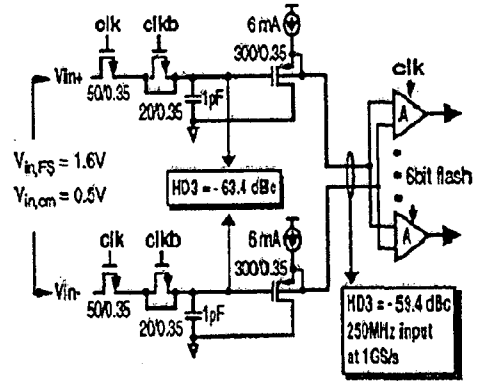


Fig.7

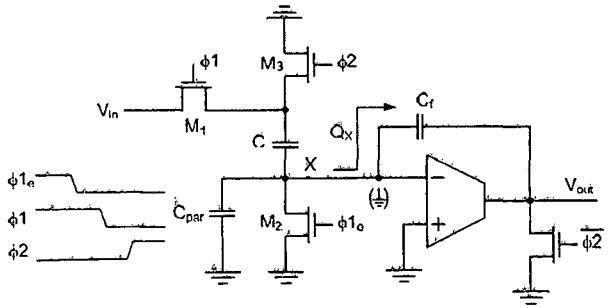
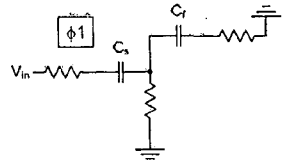
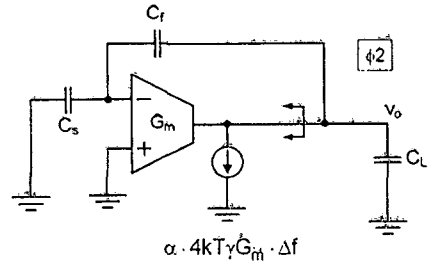


Fig.8



Noise due to switches

Fig.9a



Noise due to amplifier and switches

Fig.9b

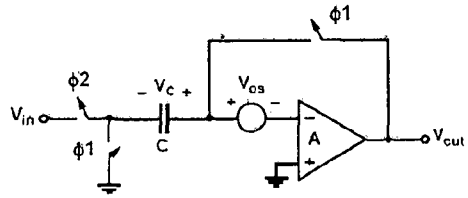


Fig. 10

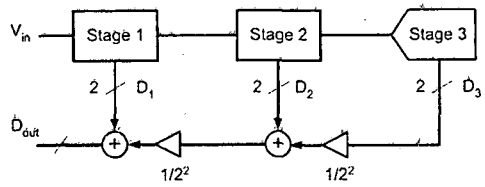


Fig. 11