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B.E. / B.Tech. (Full Time) DEGREE END SEMESTER EXAMINATIONS, NOV / DEC 2011

COMPUTER SCIENCE & ENGINEERING BRANCH

SECOND SEMESTER – (REGULATIONS 2008)

CS 9152 - Digital Principles and System Design

Time : 3 Hrs. **Max. Marks: 100**

Answer ALL Questions

PART – A (10 X 2 = 20 Marks)

1. Convert the hex number 2FB8 to binary and octal.
2. Simplify the expression Y (A,B,D) – (A' +B)(A+B+D)D'.
3. Write HDL code for a circuit specified with the Boolean expressions:
   X = A + BC + B'D and
   Y = B'C + BC'D'
4. Design a magnitude comparator that compares two one -bit numbers.
5. A multiplexer is otherwise called a data selector. Justify.
6. Draw the logic diagram of a memory cell.
7. How the indeterminate state of SR latch is eliminated by a D latch?
8. Give the excitation table of SR Flip Flop.
9. What is meant by a transition equation? Give an example.
10. What is a ripple counter? Name any two ripple counters.

PART – B (5 X 16 = 80 Marks)

11. i) Using the *Quine-McCluskey* method, obtain a simplified *sum-of- products* expression for the following Boolean function: (10)

$$f(a,b,c,d) = \Sigma (0,5,7,8,9,10,11,14,15)$$

ii) Simplify the following Boolean expression using four-variable *K*-map : (6)

$$F = x'z + w(x'y + xy') + w'xy'.$$

12.a. i) Design a combinational circuit that generates the 9's complement of a BCD digit. (8)

ii) Implement a full adder with two 4 X 1 multiplexers. (8)

(or)

b. i) Write the HDL dataflow description of a 4-bit adder-subtractor. (8)

ii) Design a BCD to Decimal decoder using the unused combinations of the BCD code as don't care conditions. (8)

13.a. i) Construct a 16 X 1 multiplexer with two 8 X 1 and one 2 X 1 multiplexers. (10)

ii) Give behavioral description in HDL of a 2-to-1 line multiplexer. (6)

(or)

b. i) Construct a 4-to-16-line decoder with five 2-to-4-line decoders with enable. (10)

ii) Design the internal logic of a PLA with three inputs (A,B,C) and two outputs (F1, F2) where the true output F1 = AB' + AC + A'B'C' and the complemented output F2 = (AC + BC)'. (6)

14.a. A sequential circuit with two D flip-flops, A and B; two inputs, x and y; and one output, z, is specified by the following next-state and output equations: (16)

$$A(t+1) = x'y + xA$$

$$B(t+1) = x'B + xA$$

$$z = B$$

i) Draw the logic diagram of the circuit.

ii) List the state table for the sequential circuit.

iii) Draw the corresponding state diagram.

(or)

b. Design a counter with T flip-flops that goes through the following binary repeated Sequence: 0,1,3,7,6,4. Show that when binary states 010 and 101 are considered as don't care conditions, the counter may not operate properly. Find a way to correct the design. (16)

15. a. Use an implication table to reduce the number of states in the state table (Table 15-a). (16)

Table 15-a

Present State	Next State		Output	
	x=0	x = 1	x=0	x = 1
a	f	b	0	0
b	d	c	0	0
c	f	e	0	0
d	g	a	1	0
e	d	c	0	0
f	f	b	1	1
g	g	h	0	1
h	g	a	1	0

(or)

b). i) Find a circuit that has no static hazards and implements the Boolean function

$F(A,B,C,D) = \Sigma\,(0,2,6,7,8,10,12)$ (6)

b). ii) Using the implication-table method, show that the state table(15-b) listed below cannot be reduced any further (10)

Table 15-b

Present State	Next state X=0	Next state X=1	Output X=0	Output X= 1
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	f	0	1
e	a	f	0	1
f	e	f	0	1