B.E. / B.Tech (Full Time) DEGREE EXAMINATION, APRIL / MAY 2013
ELECTRONICS AND COMMUNICATION ENGINEERING
EC 9038 VLSI SIGNAL PROCESSING

Time: 3 Hrs. Max.Marks: 100

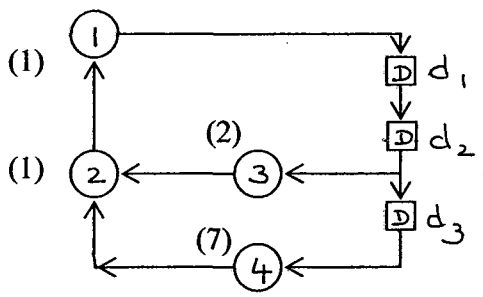
Answer All Questions

Part-A **(10 x 2 = 20 Marks)**

1. What is the difference between DFG and Dependency graph?
2. Define critical path and iteration bound.
3. Write the two rules used in unfolding algorithm.
4. What is the advantage of modified Cook-Toom's algorithm over Cook-Toom's?
5. What is algorithmic strength reduction?
6. Draw a 2x2 odd-even merge sort architecture.
7. What is numerical strength reduction?
8. What is sign extension?
9. What are the properties of CSD numbers?
10. What is clock skew?

Part-B **(5 x 16 = 80 Marks)**

11. Calculate the iteration bound using LPM algorithm for



12 (a). Unfold the equation y(n)=ay(n-5) + x(n) by a factor J=2.

OR

12(b). Obtain a 4 x 1 merge-sort circuit using 1x1 C&S units.

13(a). Construct a 2 x 2 convolution algorithm using Cook-Toom algorithm with $\beta_0 = 0$, $\beta_1 = 1$ and $\beta_2 = -1$.

OR

13(b). Design a 3-level pipelined architecture for the IIR filter y(n+1) = ay(n) + u(n).

14(a). Explain Lyon's precision multiplication.

OR

14 (b). Obtain the CSD number for the 2's complement number 0.11011101

15 (a).Explain the determination of clock period in edge triggered systems in the presence of clock skew.

OR

15 (b). What is wave pipelining and derive an expression for the clock period?

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