23/5/13

B.E. DEGREE END SEMESTER EXAMINATIONS, MAY 2013
ELECTRONICS AND COMMUNICATION ENGINEERING
FOURTH SEMESTER – (REGULATIONS 2008)
EC 9251 DIGITAL ELECTRONICS AND SYSTEM DESIGN

18

Time: 3 hr Max. Marks: 100

Answer ALL Questions

Part – A (10 x 2 = 20 Marks)

1. Realize f(A,B,C) = Σ(0,2,3,7) and g(A,B,C)= Σ (1,3,5,6) using appropriate Decoder

2. Simply the function f(A,B,C,D)= Σ(0,2,5,7,8,10,13,15) using K-map.

3. Distinguish between Mealy and Moore sequential networks.

4. Draw logic schematic of master-slave flip flop using NAND gates only.

5. Define Essential Hazard.

6. Draw a flow table showing cycle problem in asynchronous circuit.

7. Realize the functions f(A,B,C) = Σ(1,3,7) and g(A,B,C)= Σ (0,2,4,7) using appropriate ROM.

8. Compare Static RAM and Dynamic RAMs.

9. Define Noise Margin.

10. What are the applications of open collector TTL gates?

Part – B (5 x 16 = 80 Marks)

11.(i) Tabulate the PLA programming table for the three boolean functions given below. Minimize the number of product terms (8 marks)

$f_1(x,y,z) = \Sigma(1,2,4,6)$
$f_2(x,y,z) = \Sigma(0,1,6,7)$
$f_3(x,y,z) = \Sigma(1,2,3,5,7)$

ii) Draw the logic diagram of 1 bit RAM cell and use this to construct 4x4 RAM (8 marks)

12(a). Obtain simplified SOP using Quine-McClusky method for
F(A,B,C,D,E) = Σ(1,3,5,7,13,21,23,25,29,31)

(or)

12(b) Explain the design of 4 bit carry look ahead adder

13 (a). Reduce the following state table to a minimum number of states

Sl. no	Present state	Next state		Output Z	
		X=0	X=1	X=0	X=1
1	a	b	c	1	0
2	b	e	d	1	0
3	c	g	d	1	1
4	d	e	b	1	0
5	e	f	g	1	0
6	f	h	b	1	1
7	g	h	i	0	1
8	h	g	i	0	1
9	i	a	a	0	1

(or)

13(b) Design a 3 bit counter which counts in the sequence 001,011,010,110,111,101,100,001,.....

i) use clocked D flip flop

ii) What will happen if the counter is started in state 000?

14 (a). An asynchronous sequential network has two inputs x_1 and x_2 and one output Z. When the input x_1x_2 is 11, the output becomes 1 and stays 1 until the input that immediately preceded the x_1x_2 =11 occurs again, at which time the output becomes 0. When the next 11 is detected, the network performs this operation again. Example:

x_1x_2 =	00	01	10	11	00	01	11	10	11	10	01	00
Z =	0	0	0	1	1	1	1	0	1	0	0	0

The first input in the sequence is not allowed to be 11. Find a minimum row flow table

(or)

14 (b). An asynchronous sequential network is designed to capture pulses on an input line X. The network has a single input X, a reset input R and an output Z. If X change from 0 to 1 or from 1 to 0 while R is 0, then the output Z becomes 1 and remains 1 until the network is reset. Thus, if there is a pulse on the input line when R is 0, the output will become 1 to indicate the occurrence of the pulse. When R=1, Z=0. Find a minimum-row flow table

15 (a) i) Explain the working of totem-pole TTL gate. (8 marks)

ii) Draw and explain the working of DTL gate. (8 marks)

(or)

15 (b). Draw the circuit diagram and explain the working of CMOS inverter, 2 input NAND and 2 input NOR gates.

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