Roll. No.

B.E/B.Tech. (Full Time) DEGREE END SEMESTER EXAMINATION, April / May 2013

ELECTRONICS AND COMMUNICATION ENGINEERING – IV SEM

EC9255 – COMPUTER ARCHITECTURE AND ORGANIZATION

19

(REGULATION 2008)

Time: 3 hour **Max. Mark : 100**

Answer All Questions

Part – A (10 x 2 = 20 Marks)

1. List out the basic steps involved in CPU processing.
2. Draw a register-level design of a 4-bit magnitude comparator.
3. Design the role of Booth algorithm in the design of fast multipliers.
4. Differentiate spatial expansion and temporal expansion of ALU.
5. What are the advantages of microprogramming control unit against with hardwire control unit?
6. How to maximize the throughput per unit of hardware cost in the pipelining system?
7. What is meant by compaction in memory allocation?
8. What is translation look-aside buffer?
9. Differentiate RISC and CISC.
10. What is SIMD and MISD?

Part – B (5 x 16 = 80 Marks)

11.a.(i) Briefly explain the organization of IAS computer with its salient features and compare it with EDVAC computer. **(8)**

(ii) Explain the different types of addressing modes with suitable examples. **(8)**

12.a.(i) With neat sketch, design a Modified Booth Multiplier to multiply 11011101_2 x 0110110_2. **(8)**

(ii) Design and implement a 4-bit CLA. **(8)**

(OR)

12.b.(i) Explain the operation of floating point adder and also explain how it is implemented with pipeline. **(8)**

(ii) Illustrate the non-restoring division algorithm for unsigned integers. **(8)**

13.a.Design a Multiplier Control Unit using Micro programmed technique with vertical and horizontal microinstructions.

(OR)

13.b.(i) Implement a control unit to design DPU of GCD processor using classical method. **(10)**

(ii) Breifly explain about the two-level control store organization for nano programming. **(6)**

14.a.State and explain the different replacement policies used in the preemptive allocation of memory in detail.

(OR)

14.b.How does a virtual address gets translated into a physical address in segmentation with paging. Explain the use of TLB in the above concept.

15.a.(i) With a neat diagram, explain any two techniques used for Bus Arbitration Mecahnism. **(8)**

(ii) Discuss in detail about memory-mapped IO and IO-mapped IO addressing. **(8)**

(OR)

15.b.(i) With a neat sketch explain the working principle of DMA. **(10)**

(ii) List the steps involved to perform transfer of control to an interrupt handler by the CPU. **(6)**