B.E. / B.Tech.(Full Time) DEGREE END SEMESTER EXAMINATIONS, NOV / DEC 2013
ELECTRONICS AND COMMUNICATION ENGINEERING
FOURTH SEMESTER – (REGULATIONS 2008)
EC 9251 DIGITAL ELECTRONICS AND SYSTEM DESIGN

20

Time: 3 hr Max. Marks: 100

Answer ALL Questions

Part – A **(10 x 2 = 20 Marks)**

1. Convert $7FF_{16}$ into its equivalent decimal number.

2. Express F(x,y,z)=xy + x'z as product of maxterms using distributive law.

3. What is race around problem in JK FF?

4. Write the states in a 4-bit Johnson counter.

5. Define dynamic hazard.

6. Write an example flow table exhibiting non-critical race.

7. What is the procedure used for erasing an EPROM?

8. What is the difference between a PAL and PLA?

9. Draw the circuit of a 3-input DTL NAND gate.

10. What are the applications of open collector TTL gates?

Part – B **(5 x 16=80 Marks)**

11. (i) Explain Essential hazard with a suitable example. (8)
(ii) Obtain reduced primitive flow table for the pft (8)

Row	AB 00	01	11	10	Output Z
1	1	2	-	3	0
2	1	2	4	-	0
3	1	-	5	3	0
4	-	2	4	3	0
5	-	6	5	7	1
6	1	6	5	-	1
7	1	-	8	7	0
8	-	2	8	7	0

(PTO)

12(a). Simplify using tabulation method $F(A,B,C,D,E) = \sum (0,1,4,5,16,17,21,25,29)$

OR

12(b). Realize $F(w,x,y,z) = \sum (0,1,2,4,5,6,8,9,12,13,14)$ using 4-to-1 MUX with yz as control inputs and extra gates.

13(a). Design a mod-10 synchronous binary counter using JK FFs.

OR

13(b). Design a Moore circuit that examines a sequence of 1s and 0s and generates an output Z=1 for the pattern 101. Overlapping is allowed. Use D FFs.

14(a). Obtain a PLA table for realizing the Boolean expressions of difference and borrow in a Full subtractor.

OR

14(b). Explain the architecture of an FPGA.

15(a). Explain the working of a TTL open collector NAND gate.

OR

15(b). Explain the working of 2-input MOS NAND and NOR gates.

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