B.E./B.Tech.(Full Time) DEGREE END SEMESTER EXAMINATIONS, NOV / DEC 2012
ELECTRONICS AND COMMUNICATION ENGINEERING
FOURTH SEMESTER – (REGULATIONS 2008)

EC 9251 – DIGITAL ELECTRONICS AND SYSTEM DESIGN

Time: Three hours Max Marks: 100

Answer ALL Questions

PART - A (10 x 2 = 20 marks)

1. What is the BCD code for the decimal number 232.768?
2. Draw the diagram of a 1 to 4 deMUX.
3. Convert an SR FF (NOR gates) to a D-FF.
4. Distinguish between Moore and Mealy networks.
5. Define essential hazard.
6. What are the points to be followed while forming primitive flow tables?
7. What is an EEPROM?
8. What is a dynamic RAM? What are its features?
9. Define noise margin.
10. Calculate the fanout given the output current =10 mA and input current = 1 mA.

PART - B (5 x 16 = 80 marks)

11. (i) Define critical and non-critical races. (6)
    (ii) Design a hazard free asynchronous circuit that has one input X and one output Z that changes state whenever the input goes from 0 to 1. (10)

12(a). Simplify using tabulation method
$F(A,B,C,D) = \Sigma(0,1,2,3,4,6,8,9,10,11,12,14)$

Or

12(b). Design a 4 input priority encoder which includes a valid output.

13(a). Explain the working of a Master-Slave JK FF that is built using NAND gates only.

Or

13(b). Design a Mealy circuit that has one input X and one output Z where Z=1 for the input sequence 101. Overlapping is allowed. Use T FFs.

14(a). Explain the architecture of CLB and FPGA.

Or

14(b). Obtain the optimum PLA Table for the functions $f(A,B,C)=\Sigma(3,5,6,7)$ and $g(A,B,C)=\Sigma(0,2,4,7)$.

15(a). Explain the working of a Totempole TTL gate.

Or

15(b). Explain the working of MOS NOT, NAND and NOR gates.

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