18/10/13

Roll No.

B.Tech. (Full Time) DEGREE END SEMESTER EXAMINATIONS, NOV / DEC 2013

5

INFORMATION TECHNOLOGY

III SEMESTER

IT 9201 - COMPUTER ORGANIZATION

(Regulation 2008)

Time: Three Hours **Max. Marks: 100**

Answer All Questions

PART-A (10 X 2 = 20 Marks)

1. Convert the following numbers to decimals
   a. $(20.25)_{16}$
   b. $(42.5)_8$
2. Which logic name is known as universal logic?
3. Draw the logic diagram of a parity generator and parity checker.
4. What are the differences among a truth table, a state table and an excitation table?
5. How to convert serial data to parallel and parallel to serial? what type of register is needed?
6. What is meant by performance metrics?
7. What is super pipelining?
8. What do you mean by interleaved memory?
9. Define the terms: Seek time, Rotational Delay, Access time.
10. Compare interrupt I/O with DMA I/O.

PART-B (5 X 16 = 80 Marks)

11. i) Simplify the following boolean function , using five-variable maps: (8)

$$F(A, B, C, D, E) = \sum (0, 1, 4, 5, 16, 17, 21, 25, 29)$$

ii) Draw the multilevel NOR circuit for the following expression (8)

$$w(x + y + Z) + xyz$$

12. a) i)Design a binary multiplier that multiplies two 4-bit numbers. use AND gates and binary adder. (8)

ii) Design a 5-to- 32 line decoder with four 3-to-8 line decoders with enable and a 2 - to -4 line decoder. (8)

OR

b)i)Design a counter with the following repeated binary sequence:0,1,2,4,6 using D flip-flops. (8)

ii) Design a serial 2's complement circuit with a shift register and a flip-flop. (8)

13. a) i)Explain Von Neumann machine with its architecture. (10)

ii) Describe the stack frame and its importance in the assembly language. (6)

OR

b)i) Explain the important features of RISC based system architecture. (6)

ii) Describe about the Memory access instruction and addressing modes. (10)

14. a) i)Explain with a diagram the designs of a fast multiplier using carry save Adder circuit. (8)

ii) Explain in detail Booth's multiplication algorithm with examples. (8)

OR

b) i) Explain briefly about the Micro Instruction and Micro program sequencing.(10)

ii) Write short note on Hazards of pipelining. (6)

15. a) i) Describe about the direct mapping and associate mapping in the cache memory. (10)

ii) Write characteristics of I/O channels. (6)

OR

b) Describe about the Memory management unit in the virtual memory and its address translation. (16)

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