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**B.E/B.TECH DEGREE END SEMESTER EXAMINATIONS, NOVEMBER 2013**

**INFORMATION TECHNOLOGY**

**SEVENTH SEMESTER – REGULATION 2008**

**IT9025 ROUTERS AND NETWORK PROCESSORS (ELECTIVE)**

**Time: 3 hrs** **Max.Marks:100**

**Answer All Questions**

**Part – A (10X2 = 20 Marks)**

1. What is the need for static routes? What is the role of Administrative Distance in static routes?
2. Differentiate conventional Shortest Path First (SPF) routing and Traffic Engineering.
3. What is the role of a switching fabric in a router?
4. Consider the following two sets of mappings.
   a. classification: packet → flow forwarding: flow → packet disposition
   b. forwarding: destination address → (next_hop, interface)

   Match the above two mappings to connectionless network and connection-oriented network.
5. List down the various Ingress processing functions.
6. What is the importance of clock rate in choosing between pipeline architecture and parallel architecture?
7. Draw the diagram that illustrates fan out in a processor hierarchy.
8. Write short notes on the tradeoff: Backward Compatibility Vs Architectural Advances
9. Mention the advantages and disadvantages of ASIC coprocessors.
10. How many embedded RISC processors and programmable packet processors are available in IXP1200 network processor?

**Part – B (5X16 = 80 Marks)**

11. i. Discuss the major features of RIP and the packet format of RIPv1. (8)
    ii. Discuss the autonomous systems and the role played by BGP in autonomous systems. (8)

12a. i. Explain Basic Queuing, Priority Queuing, Weighted Round Robin and Weighted Fair Queuing and discuss their performance. (10)

ii. Explain Tail Drop, Random Early Detection and Early Packet Discard mechanisms briefly. (6)

(OR)

12b. i. Explain the Bridge Forwarding Algorithm. (6)

ii. Explain the IP Datagram Fragmentation algorithm. (10)

13a. i. Explain the procedure of assigning functionality to the processor hierarchy with the diagram that illustrates the packet flow through the processor hierarchy. (8)

ii. Consider a second generation network system that forwards IP datagrams. If the system has 16 interfaces that each connect to an OC-48 line, what aggregate bandwidth is needed on an internal mechanism that interconnects the 16 interfaces? Assume a 4-octet identifier is transferred with each packet. (8)

(OR)

13b. i. Explain the crossbar switching fabric and the basic queuing followed in the crossbar switching fabric. (8)

ii. Let O be the number of instructions executed per octet, and P be the number of instructions per packet. What ratio of P/O makes per packet overhead dominate for ATM cells? for minimum size datagrams? for maximum size datagrams? Assume each datagram carries a TCP segment. (8)

14a. i. Explain the scaling of a Network processor with Content Addressable Memory. (8)

ii. Discuss the procedure of packet classification using CAM. (8)

(OR)

14b. i. Explain the architecture of Agere Multi-Chip Pipeline network processor in terms of FFP, RSP and ASI in detail with a neat diagram. (10)

ii. Explain the Cisco's Pipeline of Homogeneous Processors briefly. (6)

15a. i. Discuss the external connections and internal components of Intel's IXP1200 network processor. (8)

ii. Explain the processor hierarchy and memory hierarchy of Intel's IXP 1200 network processor. (8)

(OR)

15b. Explain the various hardware mechanisms, techniques and architectures to overcome the problem of single CPU bottleneck. (16)

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