19/11/13

incomplete

B.E/B.Tech (Full time) DEGREE END SEMESTER EXAMINATIONS, NOV/DEC 2013

IT

III Semester

IT8301- Computer Organization

(Regulation 2012)

Time: 3 hr Max.Mark:100

Answer ALL Questions

PART A **10x2=20**

1. Given the two signed binary numbers X = 11101111 and Y = 10011101, perform X-Y and Y-X using 2's complement code.
2. Simplify the Function F= A'BC + A'B'D + A'CD and find the complement of F using Boolean Algebra.
3. Design a 16X1 MUX using 4X1 MUXs. Use symbols for MUXs.
4. List four applications of shift registers.
5. Classify the instructions based on the no. of operands in the instruction. Give example to each one.
6. Distinguish RISC and CISC processors
7. List the advantages and disadvantages of hardwired and microprogrammed control.
8. What is ideal the CPI (clock cycles per instruction) in pipelined processors?
9. Differentiate SRAM and DRAM memories.
10. Define memory mapped I/O.

PART B **5x16=80**

11. (i)Simplify the given Boolean function in SOP form using K map.
F(A,B,C,D)=B'C'D'+A'BC'D'+ABC'D'+A'B'CD+AB'CD+A'B'CD'+A'BCD'+ACD' (8)

(ii)Simplify the given Boolean function in POS form using K-map

F(P,Q,R,S) = Π M(0,1,4,7,8,10,12,15) and d(2,6,11) (8)

12. (a)(i)A conference hall has two doors and one window with sensors. A control switch is used to control them as follows. If control switch is OFF , the doors and window can be opened and the A/C is kept OFF. If it is ON and the doors and windows are closed, then A/C is switched ON. If the control switch is ON with doors closed but window opened, then A/C is switched OFF. If any one or both the doors opened with control switch ON, then A/C is OFF and a buzzer is ON. Design a logic circuit to implement the above. Assume ON as logic 1 and OFF as logic 0. When door or window is closed, the sensor signal is logic 1. Otherwise it is logic 0 (10)

(ii) Implement the following Boolean functions using a 4:16 decoder
F1(W,X,Y,Z) = $\sum$ m(0,1,4,7,8,10,12,15) and F2(W,X,Y,Z) = $\sum$ m(2,3,5,7,10,11,13). Select any one function at the output using a 2x1 multiplexer. (6)

14. (a)(i)List the sequence of elementary operations carried out to execute a complete instruction. (4)

(ii) Draw the datapath with single bus structure. Write the control sequences for the following instructions.

SUB (R1), R5 and Branch<0, +16(PC) (2+5+5)

(OR)

(b)(i)What is hazard in pipelined processor? List the types of hazards. Explain the techniques to reduce effect of these hazards. (12)

(ii)Consider the following sequence of instructions

Sub #34, R0, R2
Add R0, R1, R3
Xor R2, R3, R4

are executed using four stage pipelined computer. Draw the pipeline diagram describing the operation performed by each stage during each of clock cycle (4)

15. (a)(i)Explain how can you achieve a larger memory using smaller memory ICs with an example. (8)

(ii)A byte-addressable computer has a small data cache capable of holding eight 32-bit words. Each cache block consists of one 32-bit word. The processor reads the following hex addresses in sequence:

8D00, 8D04, 8D00, 8D0C, 8DF4, 8D04, 8D18, 8D2C, 8D28, 8DF4

This pattern is repeated for four times. Show the contents of the cache at the end of each pass through this loop if direct mapped cache is used. Compute hit rate. Assume that the cache is initially empty. (8)

(OR)

(b)Discuss in detail about Interrupts and Direct Memory Access associated with computers. (8+8)