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B.E. / B.Tech ARREAR EXAMINATIONS, NOV / DEC 2011

ELECTRONICS AND COMMUNICATION ENGINEERING BRANCH

SIXTH SEMESTER

(REGULATION 2008)

EC 9355 - DIGITAL VLSI

Time: 3 Hours Max.marks: 100

PART-A (10x2=20 Marks)

1. Consider an NMOS transistor with the biasing condition given by V_{GS}=2.5V, V_{DS} =0.5V.Assume the device dimension W/L to be 2/1. Determine the drain current I_D. Use the following device parameters for calculation, Kn=115μA/V^2,V_{T0}=0.43V, λ =0.1V^{-1},VDSAT=0.63V.
2. Consider an inverter that operates with a supply voltage of 2.5V. Assume the load capacitance of the inverter as 6fF.If the propagation delay of the inverter is 35ps, compute the dynamic power dissipation, when the inverter is switched at the maximum possible frequency.
3. Size the NMOS and PMOS transistor for the circuit given in Fig.1 such that the output resistance is same as that of an inverter with an NMOS W/L=3 and PMOS W/L=6.

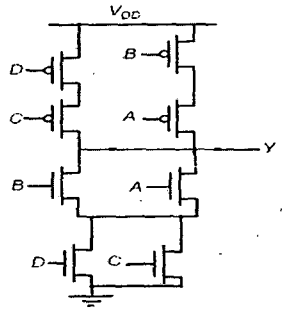

Figure 1

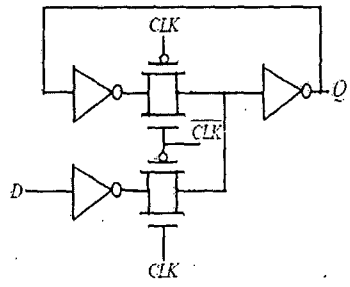

Figure 2

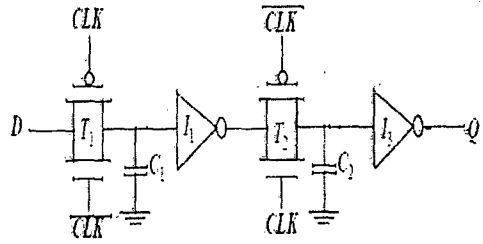

Figure 3

4. Implement the Boolean logic function F=$\overline{ABC} + A\bar{C}$ in DCVSL.
5. What type of latch is shown in Fig.2 and justify with reason.
6. Give the setup time of the edge triggered register given in Fig3.
7. Give the critical path delay for a four bit ripple carry adder.
8. Draw the circuit of one bit programmable shifter.
9. Give the configuration of Xilinx SRAM cell to program the interconnections.
10. Show the realization of the Boolean logic function F=$\bar{A}.B.\bar{C} + A.\bar{B}.\bar{C} + \bar{B}.C$ using multiplexers as function generators.

PART B (5x16=80 MARKS)

11.(i) Derive the VTC of the inverter. Draw and Mark significant points on the VTC. **(8)**

(ii) Derive switching threshold of an inverter and state how the relative sizing of NMOS and PMOS devices helps in shifting the switching threshold. **(8)**

12.(a) Consider the pseudo NMOS circuit given in Fig.4. Use the following device parameters for calculation NMOS: $K_n=115\mu A/V^2$, $V_{T0}=0.43V$, $\lambda=0.1V^{-1}$, VDSAT=0.63V
PMOS: $K_p=-30\mu A/V^2$, $V_{T0}=-0.4V$, $\lambda=0.1V^{-1}$, VDSAT= -1V.

i. Determine the switching threshold for the given circuit. **(4)**
ii. What is V_{OH} and V_{OL} of this circuit? **(4)**
iii. Determine V_{OH} and V_{OL} if only one input is high. **(4)**
iv. What is the static power dissipation if each input turns on with statistically independent probability of 0.2 ? **(4)**

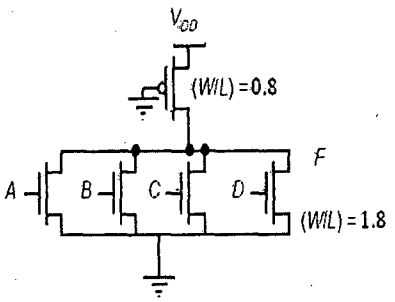

Figure 4

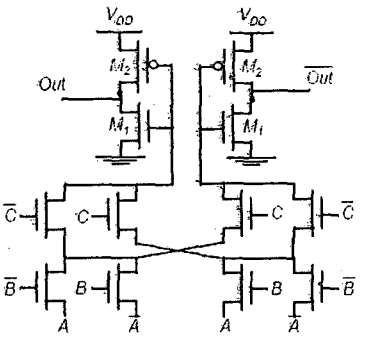

Figure 5

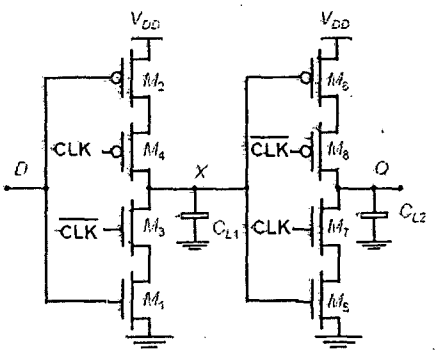

Figure 6

OR

12.(b)(i) Give 2 design issues in dynamic logic circuit. Give circuit techniques to minimize those issues. **(8)**

(ii) Give the Boolean logic expression for *out* and $\overline{out}$ of the circuit given in Fig.5. Explain why this circuit has static power dissipation. Give an alternate circuit technique to minimize the static power dissipation. **(8)**

13.(a) Consider the C^2MOS logic style register given in Fig.6.

i. State the type of edge triggered register with justification. **(4)**
ii. Why this circuit is insensitive to clock overlap? **(8)**
iii. Derive a dual edge triggered register from this C^2MOS logic style register. **(4)**

OR

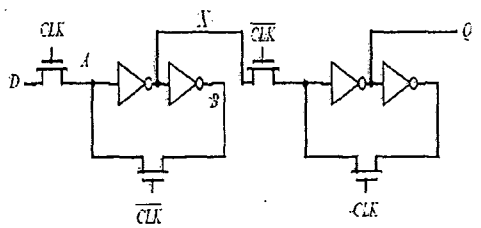

Figure 7

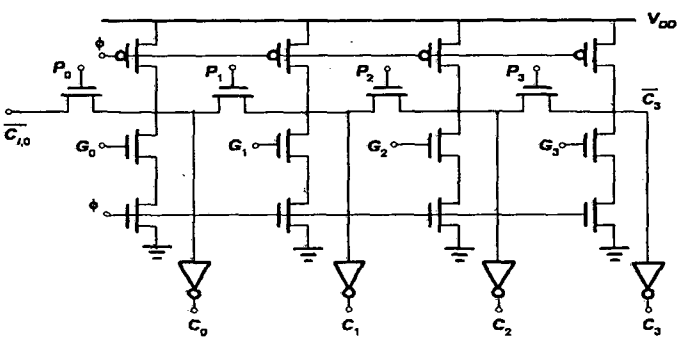

Figure 8

13.(b) Consider an edge triggered register circuit given in Fig.7.

i. State the type of edge triggered register with justification. **(4)**

ii. Determine the setup time, hold time and CLK to Q delay of this register **(6)**

iii. Give the issues related to CLK and $\overline{CLK}$ overlap and give alternate circuit technique to minimize this overlap **(6)**

14.(a)(i) Derive the carry generation circuit for a 4-bit carry look ahead adder. **(8)**

(ii) Derive the critical path delay in a carry bypass adder and show that the critical path delay can be minimized using linear carry select adder. **(8)**

OR

14.(b)(i) The circuit given in Fig. 8 is a carry generation circuit. What are P and G signals? Determine the expression for carry generation. Derive the critical path delay of this circuit. **(8)**

(ii) Give the architecture of a 4X2 array multiplier and derive its critical path delay. **(8)**

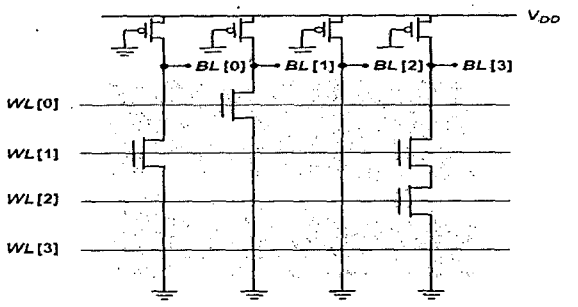

Figure 9

15.(a)(i) Explain the architecture of CLB of XILINX XC4000 device and the interconnect architecture. **(10)**

(ii) Explain how an ACTEL antifuse is used as a programmable interconnect **(6)**

OR

15.(b)(i) Give the data content stored in the MOS NAND ROM cell shown in Fig. 9. **(4)**

(ii) Draw a six transistor SRAM cell and derive the transistor device dimension ratios for read and write operations **(12)**
