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**B.E/B.Tech (Full Time) DEGREE END SEMESTER EXAMINATIONS, NOV/DEC 2011**  
**ELECTRONICS AND COMMUNICATION BRANCH**  
**SIXTH SEMESTER (REGULATION 2008)**  
**EC 9078 EMBEDDED AND REAL TIME SYSTEMS**

38

Time : 3 Hrs

Max. Mark :100

Answer ALL Questions**PART-A****(10 x 2 = 20 Marks)**

1. What are the fields present in a sample requirement form?
2. Write an ARM assembly code for the C assignment,  $y=(c-d) + (e-f)$ .
3. Draw the elements of the ARM AMBA bus system.
4. What is meant by instruction pipelining?
5. Define "priority inversion".
6. What is meant by "scheduling overhead"?
7. What is the need to have a multiprocessor embedded system?
8. Draw the CAN data frame format.
9. What are the two ways by which a software modem can be tested?
10. List out the levels in the designing of an embedded computing system.

**PART-B****(5 x 16 = 80 Marks)**

11. With neat sketches, explain the hardware and software architecture of a settop box. (16)

- 12.a)(i) Write an ARM assembly code that implements the following C conditional:

```

if (x-y < 3) {
    a = b-c;
    x = 1;
}
else {
    y = 1;
    d = e + f + g;
}

```

(8)

- (ii) Draw a UML sequence diagram for copying characters from an input to an output device using busy wait I/O. The diagram should include the two devices and two busy-wait I/O handlers. (8)

**(OR)**

- 12.b)(i) With suitable examples, briefly explain about the compulsory miss, capacity miss and conflict miss. (8)

- (ii) Draw a state diagram for a behaviour that sends the command bits on the track. The machine should generate the address, generate the correct message type, include the parameters and generate the error correcting code (ECC). (8)

- 13.a)(i) With a neat diagram of a resistive touchscreen, explain its working principle in detail. (8)

- (ii) Find the cyclomatic complexity of the CDFG for the code fragment given:

```

if (a < b) {
    if (c < d)
        x = 1;
    else
        x = 2;
} else {
    if (e < f)
        x = 3;
    else
        x = 4;
}

```

(8)

**(OR)****(P.T.O)**

13.b) What is meant by "loop optimization? Explain with suitable example in detail about the three important techniques in optimizing the loops. (16)

14.a)(i) Discuss in detail about the timing requirements with respect to release time and deadline for different types of processes. (8)

(ii) With neat sketches, explain in detail about shared memory communication. (8)

(OR)

14.b) Using Earliest Deadline First (EDF) policy, schedule the periodic process shown below:

Process	CPU Time	Deadline
P1	1	3
P2	1	4
P3	2	8

Compute the schedule for an interval equal to the hyperperiod of the process. Assume the time starts at  $t=0$ . (16)

15.a) What is an I<sup>2</sup>C bus? With the help of state transition graph and control word formats, briefly explain how the data transaction is taking place using the I<sup>2</sup>C bus? (16)

(OR)

15.b)(i) Explain briefly about the cache updating problem in an accelerated system with a neat diagram. (8)

(ii) Explain about fixed priority arbitration scheme and fair priority arbitration scheme with an example for each. (8)

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