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B.E. / B.Tech DEGREE END SEMESTER EXAMINATION, NOV/DEC 2011
Electronics and Communication Engineering Branch
VII Semester - (Regulations 2004)
EC 472 – VLSI DESIGN

Time: 3 Hours **Max.marks: 100**

Answer ALL questions **PART-A** **(10 x 2=20 marks)**

1. What is meant by body effect?
2. What are the types of scaling?
3. Draw the stick diagram of two input NOR gate.
4. Define Power delay product and energy delay product.
5. Considering the input signal statistics, derive the transition probabilities for two input AND and NOR gate.
6. What are the important timing parameters of sequential circuit?
7. What is a data path circuit?
8. Implement carry output of full adder using CMOS logic.
9. Differentiate hard and soft macro.
10. What is an antifuse?

Part B **(5 x 16 = 80)**

11. i) Implement the sum output of full adder using CMOS and Dynamic logic. (8)
ii) Derive the propagation delay of 4 input NAND gate for 1 to 0 transition, using elmore's constant. (8)

12. a i. Derive for the drain current of a MOS device in various regions of operation (10)
ii. Discuss the secondary effects of MOS device. (6)

(OR)

b. i. Draw and explain the Voltage Transfer characteristics (VTC) of CMOS inverter. (10)
ii. What is the effect of scaling on MOS devices (6)

13. a. i. Discuss the meta-stable property of bi-stable circuit. (6)
ii. Implement dynamic edge triggered register and discuss its timing properties. (10)

(OR)

b. i. Explain the structure of 4 X 4 ROM cell array. (6)
ii. With neat block diagram, explain the architecture of contents-addressable memory. (10)

14. a. i. Derive the worst case delay of linear carry select adder and find the delay for 12-bit adder. (8)
ii. Implement propagate and generate signals of adder using dynamic logic. (8)

(OR)

b. i. Explain Modified Booth's Recoding algorithm for multiplication of two 8-bit numbers. (6)
ii. Explain the operation of barrel shifter with the structural diagram (10)

15. a. i. Briefly explain semicustom design flow. (6)
ii. Draw the internal architecture of any one type of FPGA. Discuss its features. (10)

(OR)

b.i. Briefly explain about Programmable Interconnects. (10)
ii. List the features of cell based programmable logic and explain any one type of logic cell. (6)