Dept. of ECE CEG Campus, Anna University
B.E (ECE) (VII) Semester (FT), End Semester Examination Nov 2011
EC 9075 CMOS Analog IC Design I: Building Blocks
Answer All Questions

Note 1: For all questions ignore the body effect
Note 2: For all questions, by default, assume all transistors are in saturation.
Note 3: In some questions, you can use your judgment and ignore r_{ds}, the output impedance of the transistors if required.

Part A (2x10=20).

Q1. Give the expression for the differential voltage gain of the circuit shown in Fig.1
Q2. Give the expression for the differential voltage gain for the circuit shown in Fig.2
Q3. Give the expression for the voltage gain of the circuit shown in Fig.3
Q4. Consider the two possible open loop transfer functions given below and indicate which one is more preferable from stability point of view when used in a feedback amplifier configuration. Justify.

$A_{OL1} = (1+jf/f_z)/\{(1+jf/f_{p1})(1+jf/f_{p2})\}$ or $A_{OL2} = \{1-jf/f_z)/\{(1+jf/f_{p1})(1+jf/f_{p2})\}$; where $f_{p1}<f_z<f_{p2}$

Q5. Write down the expression for the differential gain of the circuit shown in Fig.4.
Q6. Derive the expression for the small signal output impedance of the source follower shown in Fig. 5
Q7. Explain what the expression kT/C represents and state its units.
.Q8. Give the expression for the UGB of the amplifier shown in Fig.6
Q9. Give the expression for the gain Vout/Vin for the circuit shown in Fig.7
Q10. Give the expression for the UGB of the circuit shown in Fig.8

Part B (5x16=80).

Q11. Consider Fig.9. The convention used is such that if $V_{in2} > V_{in1}$, then current flow from the transconductor is in the direction of the arrow.

(i) What is the DC open loop gain A_{V0} of the circuit shown in Fig. 9. (2)
(ii) Give the expression for unity gain frequency(UGB). Does your expression correspond to open loop or closed loop case. Does your UGB depend on the nondominant pole. If your answer is 'yes', explain how, if it 'no', explain why not. (4)
(iii) Give the open loop transfer function of this circuit. (4)
(iv) Explain with justification, how you would select the non dominant pole.(4)
(v) Redraw this diagram in your answer sheet and show how you would use it as a unity gain buffer.(2)

Q12.a (i) Obtain the expression for the gain and output impedance for the circuit in Fig.10. Output is to be taken at the drain of M2 and a suitable drain bias current source is assumed and not shown in the figure. You should start from first principles with the simplified equivalent circuit. including r_0 of each transistor. (6)

(ii) Using your answer to part (i) above, write down the expression for the small signal output impedance Rout of the circuit shown in Fig.11. (5)

(iii) Write down the expression for the small signal output impedance of the circuit shown in Fig.12. (5)

OR

Q12. b (i) Explain if the circuit shown in Fig.13 is a single stage or two stage amplifier. Redraw the circuit in your answer sheet and mark the polarities to correctly define the differential input voltage and the corresponding differential output voltages. (4)

(ii) Explain the need for common mode feedback (2)

(iii) How is the common mode voltage sensed and how is it stabilized. What is the final output common mode voltage. (6)

(iv) State whether the circuit employs positive, negative or no feedback for the common mode output voltage. Justify. (2)

(v) State whether the circuit employs positive, negative or no feedback for the differential mode output voltage. Justify (2)

Q13. a.(i) Consider the circuit in Fig.14. Assume all transistors have same Vt and that all are biased with the same overdrive V_{od}. Write down the expressions for the maximum and minimum permissible voltages for which all (both input and output) transistors will be in saturation. (8)

(ii) Consider the circuit in Fig.15 along with the data given. Determine the slew rates (both high to low and low to high) for this circuit. State which transistors will be conducting for the corresponding high to low and low to high transitions. (8)

OR

Q13. b(i) In Fig. 16 below, determine the expression for the equivalent input noise voltage v_n. What could be the possible units for this. You must consider the 1/f noise the transistor. (6)

(ii) For the circuit in Fig.17, determine the expression for low frequency closed loop gain and closed loop input impedance. (10)

Q14. a(i) Consider the circuit in Fig.18. Write down the expression for the impedance measured at the drain node of M4. Assuming that all transistors have the same threshold voltage and that they are sized so that their overdrive voltages are identical, determine the smallest possible output voltage at the drain of M4. (8)

(iii). Consider the circuit of Fig. 19 and write down the expression for the ratio I_{out}/I_{ref} in terms of the W/L ratios of the various transistors. Give the expression for the maximum and minimum output voltages possible. What is the expression for the output impedance of this current mirror circuit. (8)

OR

Q14. b(i) Consider the differential amplifier circuit shown in Fig.20 and the corresponding drain current versus differential input voltage graph in Fig. 21. Determine the expression for +/- ΔVin, which as per the graph in Fig.22, represents the input differential input voltage at which the currents saturate. This expression should be given in terms of I_{SS} and the device parameters of the transistors. (10)

(ii) Consider the circuit in Fig.22. In this circuit, 0.8(Iss/2) represents the current through the transistors M5 and M6. Write down the expressions for the differential gain of this amplifier. What is the need for the transistors M5 and M6.(6)

Q15. a Consider the circuits in Fig.23, Fig.24, and Fig.25. Write down, in the form a table, the expressions for gain, output impedance, minimum and maximum output voltages for each of these circuits. (16)

OR

Q15.b Using symmetry considerations, derive the expressions for the small signal differential gain, and common mode gain, and CMRR of the circuit shown in Fig.26

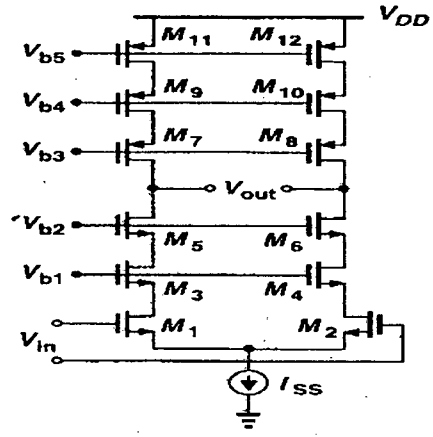

Fig.1

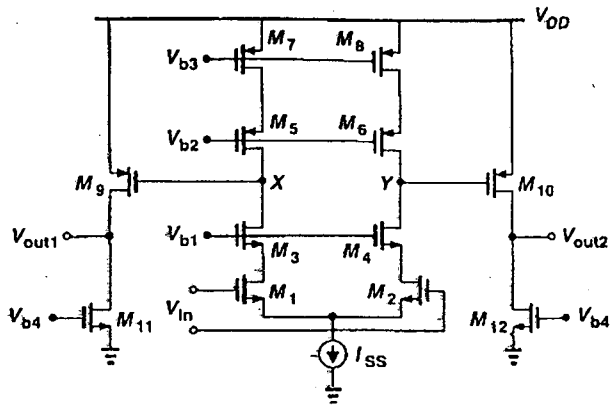

Fig.2

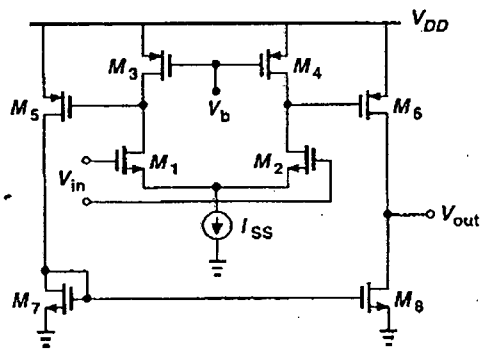

Fig.3

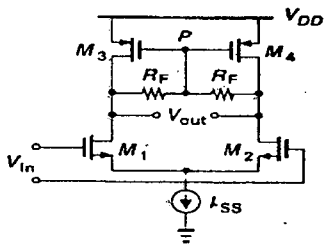

Fig.4

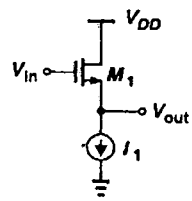

Fig.5

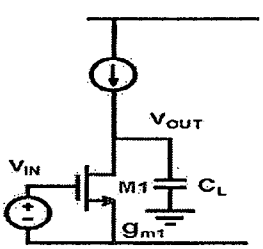

Fig.6

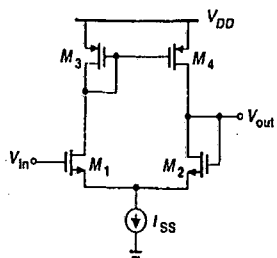

Fig.7

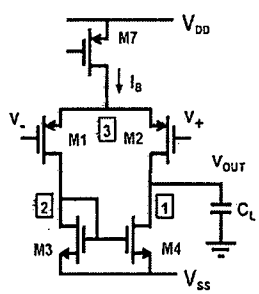

Fig.8

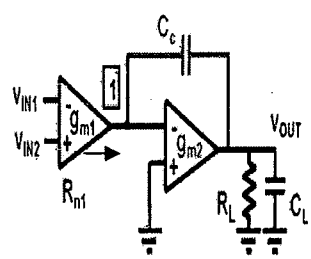

Fig.9

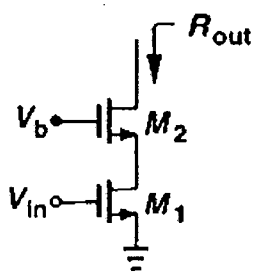

Fig.10

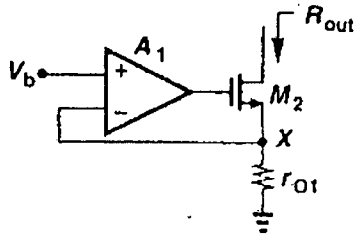

Fig.11

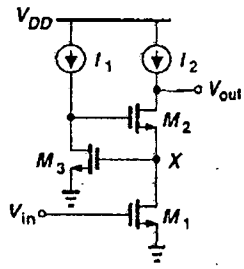

Fig.12

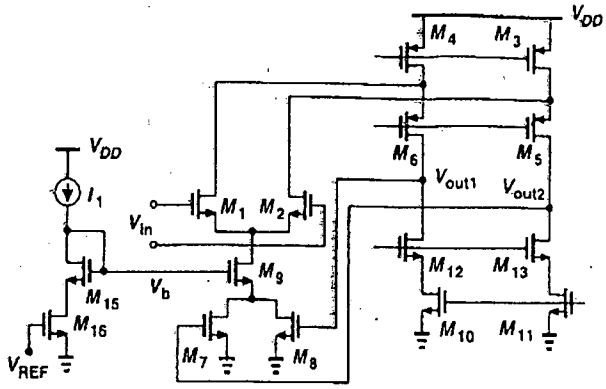

Fig.13

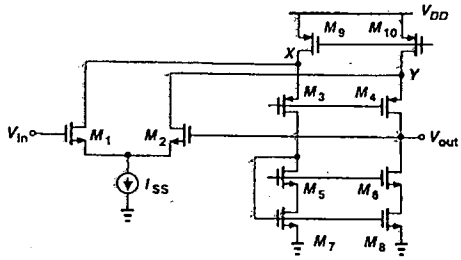

Fig.14

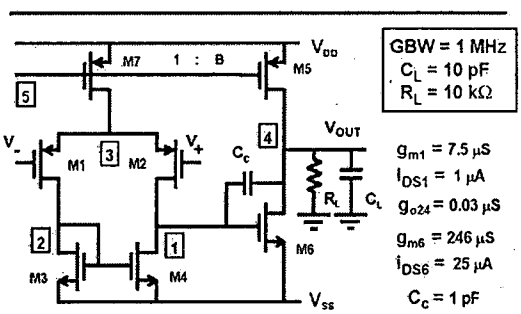

Fig.15

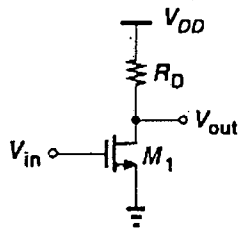

Fig.16

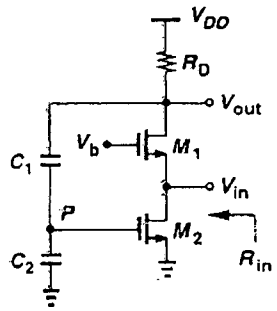

Fig.17

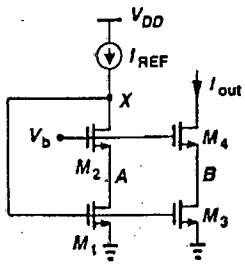

Fig.18

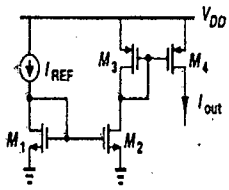

Fig.19

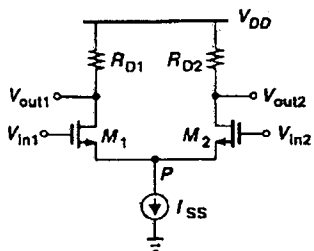

Fig.20

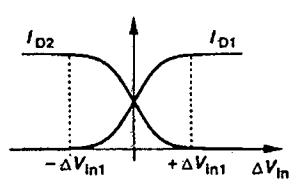

Fig.21

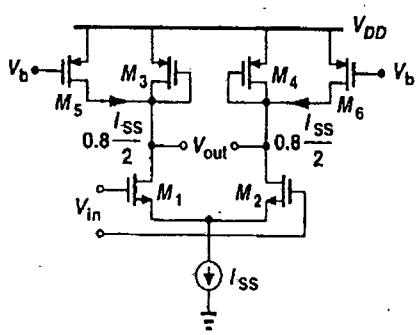

Fig.22

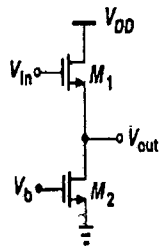

Fig.23

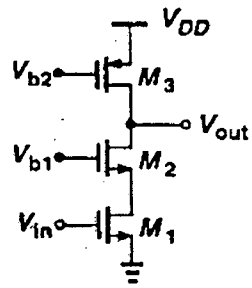

Fig.24

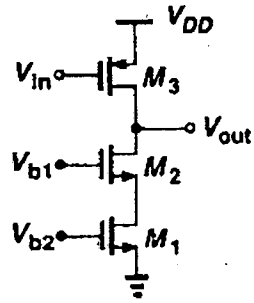

Fig.25

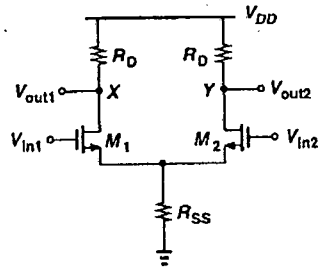

Fig.26