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B.E. / B.Tech (Full Time) DEGREE END SEMESTER EXAMINATIONS, NOV / DEC 2011

Electronics and Communication Engineering Branch

54

EIGHT SEMESTER

EC 514 – CAD for VLSI

(REGULATIONS 2004)

Time: 3 Hours

Max. Marks: 100

Answer All Questions

Part-A

(10 x 2 = 20 Marks)

- 1) Define the term clique.
- 2) Differentiate the data types and the data structures.
- 3) How is the placement algorithms grouped?
- 4) Write short notes on problem formulation.
- 5) Give the major objectives of floorplanning process.
- 6) Define area routing.
- 7) List the Various Kinds of simulation process.
- 8) Prepare the comparison table between gate-level modeling and switch-level modeling.
- 9) What is meant by high level transformations?
- 10) Why the high level synthesis model is necessary for hardware implementation process?

Part-B

(5 x 16 = 80 Marks)

11)

- (a) Describe in detail about the various VLSI design automation tools in the physical design cycle. (16)

12)

- (a) What is meant by "minimal spanning tree"? Explain the "Prim's" and "Kruskal's" algorithm to construct it. (16)

(or)

- (b) Explain in detail steps:-

- (i) Informal problem formulation. (4)
- (ii) Graph-theoretical formulation. (12)

13)

(a) Describe in detail about the various channel routing models (16)

(or)

(b) Explain in detail about the Rectilinear Steiner-tree construction in global routing technique. (16)

14)

(a) Describe in detail about the ROBDD principles, implementation, construction and manipulation technique. (16)

(or)

(b) Explain in detail about the two-level logic-synthesis. (16)

15.

(a) Mention the various hardware components that can be used by a system for the processing of high level synthesis. (16)

(or)

(b) Describe the Force directed scheduling algorithm. (16)