18/10/13

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End Semester Examinations - Nov/Dec 2013 (R 2002/2004/2008)

BE(Full Time) – III Semester- Electrical and Electronics Engineering

College of Engineering, Anna University,Chennai-600 025

Time : 3 Hours | EE 273/ EE 9204- Digital System Design & EE333 Digital Systems | Max Marks :100

Answer ALL Questions

Part –A **10 X 2 = 20**

1. Simplify using Boolean rules : f(X,Y,Z) = (X + Y + XY)(X+Z)
2. (i) Given (0110-0001-1001) in standard BCD. Find its decimal equivalent. (ii) How many digits in binary notation are required for the decimal number 17 ?
3. What are universal gates? Why are they called so?
4. Realise an inverter using a three input NAND gate.
5. Draw the logic diagram of a 4 X 1 multiplxer.
6. Use a 2 X 4 PAL and implement the logic function F = AB + A'B'
7. (i) How many flip flops are required to build a mod-19 counter? (ii) A synchronous sequential circuit has 8 (Eight) states. How many flip flops are required to design the circuit?
8. Differentiate combinational logic circuits and sequential logic circuits
9. Construct a divide by 16 ripple up counter.
10. What is meant by critical and non–critical race conditions in asynchronous sequential circuits ?

Part-B **5 x 16 =80**

11. (i) Convert the number $[748]_{10}$ to base 4, base 12, base 16 and base 32 (4)

    (ii) Simplify the given Boolean function using K map. f(A,B,C,D) = Σm(3,7,11,13,14,15)

    Realise the reduced expression using NAND gates. (8)

    (iii) Find the compiement of the Boolean expression
    f(A,B,C,D) = (A B'+ C)(A' + D)(C+D) (4)

12 (a) (i) Design a logic circuit with three inputs and one output. The output is equal to logic- 1 when the binary value of the input is 2,3,6 and 7. The output is logic-0 otherwise.

    (a) Write down the truth table for the circuit (3)

    (b) Write down the reduced Boolean equation that describes the circuit (2)

    (c) Draw the logic diagram using AND,OR and Invert gates. (3)

    (ii) Design a full adder circuit. (8)

(OR)

12(b) (i) A combinational circuit produces the binary sum of two 2-bit numbers, $x_1\ x_0$ and $y_1\ y_0$ The outputs are C,S_1 and S_0.

(a) Write down the truth table for the circuit (3)

(b) Write down the reduced Boolean equation that describes the circuit (2)

(c) Draw the logic diagram using AND,OR and Invert gates. (3)

(ii) Using the Quine- Mccluskey method obtain all the prime implicants and the essential prime implicants of the given Boolean function . Draw the logic diagram for the reduced expression $F(x_1,x_2,x_3,x_4) = \sum (0,2,3,4,8,10,12,13,14)$ (8)

13(a) (i) A combinational circuit is defined by the following Boolean functions. Design the circuit wih decoder and gates.

$F_1(x, y, z) = x' y' z' + xz$

$F_2(x, y, z) = x y' z' + x' y$ (8)

(ii) Draw a ROM to implement the Boolean functions

$F_1(A,B,C,D) = ABCD+AB'CD'+ A'BC'D+ABC'D'$

$F_2(A,B,C,D) = AB'+A'B$ (8)

(OR)

13(b) (i) A combinational circuit is defined by the following Boolean functions. Design the circuit wih 4 X 1 multiplexers. The binary variables x and y are connected to the selection lines S_1 and S_0 respectively.

$F_1(x, y, z) = x' y' z' + xz$

$F_2(x, y, z) = x y' z' + x' y$ (12)

(ii) Give a brief description about PAL. (4)

14(a) A sequential circuit has three D flip flops A,B,C and one input x. It is described by the following flip flop input functions $D_A = (B C)x + B'C' x'$; $D_B = A$; $D_C = B$. The output $y = AB + C x$. Derive the state table and draw the state diagram.

(OR)

14(b) (i) Design a synchronous decade counter. Use T flip flops for realisation. (8)

(ii) Derive the characteristic equation and excitation table of S-R Flip flop. (8)

15(a) Design a half adder. Develop a VHDL code for the half adder. (16).

(OR)

15(b) (i) Explain the difference between asynchronous and synchronous sequential circuits (3)

(ii) Define Fundamental mode operation (3)

(iii) An asynchronous sequential circuit is described by the following excitation and output functions.

$Y = x_1 x_2' + (x_1 + x_2')\, y$; $z = y$

Draw the logic diagram and derive the transition table and output map (4+3+3)