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Roll No. | | | | | | | | | | |

B.E / B.Tech (Full Time) DEGREE END SEMESTER EXAMINATIONS, NOV / DEC 2013

Electrical and Electronics Engineering (EEE)

Semester 6

EE 9028 Computer Architecture

(Regulation 2008)

Time 3 hours Maximum marks 100

Answer All Questions

PART A – (10 x 2 = 20 marks)

1. What are the different buses possible in a computer?
2. What are the different fields of an instruction of a model computer
3. What is the advantage of micro programmed control over hard wired control?
4. What is pipelining in a computer?
5. What is CISC?
6. What is a UART? What is it used for?
7. What is DMA?
8. What is memory mapped I/O?
9. What is cycle stealing?
10. What is memory interleaving?

PART B – (5 x 16 = 80 marks)

11 a i) Give the flow chart for the instruction cycle of a model computer whereby it differentiates between I/O, Register, Direct and Indirect instructions. Explain it briefly 12

11 a ii) How does the model computer keep track of the return address and gets it back on branching from one place to the other? 4

12 a) Explain the various addressing modes of a model computer with examples 16

OR

12 b i) Explain the working of a sequencer of a micro-programmed control 12

12 b ii) If a control memory is ranging from 0 to 512 for storing micro programs (for various operations) and if there are 32 different operations to be micro programmed, suggest a proper mapping function. Justify your suggestion 4

P T O

13 a i) explain the hardware implementation of multiplication of signed magnitude data. Hence multiply 22 by 3 showing the values in different registers and flag bits in the status register 16

OR

13 b i) Give the working principle behind Booth Multiplication algorithm. Hence do 30 x 14 showing the contents in the various registers. 16

14 a i) Explain the Strobe controlled Asynchronous Data transfer. 8

14 a ii) Draw the block diagram for the asynchronous communication interface. 8

OR

14 b i) Explain the CPU program to input data with a flow chart. 10

14 b ii) Give the flow chart for the daisy chaining of priority interrupt 6

15 a) give the different mappings of the cache memory and explain with a comparative study. 16

(OR)

15 b) In relation to paging, explain page table, page fault, physical address, logical address. 16